ATM5/e Series Hardware

Design Guide

SUMMARY: This document describes how to implement hardware designs with the ATM5/e Wireless SoC Series, including layout guidelines, RF matching guidelines, digital I/O connections, and PMU (Power Management Unit) configuration.

Atmosic™

ATM5/e Series Hardware Design Guide
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Acronyms and Abbreviations

Acronyms	Definition
ATM5/e	ATM53/e ATM52
ATM53/e	ATM53 ATM53e
ATM53	ATM5305
ATM53e	ATM5305e
ATM52	ATM5205
EVB	Evaluation Board
EVK	Evaluation Kit
NVM	Non-Volatile Memory
PMU	Power Management Unit
RAM	Random Access Memory
ROM	Read-Only Memory
SoC	System-on-Chip

1. Overview

The ATM5/e Wireless SoC Series is part of a family of extreme low-power Bluetooth® SoC devices. This SoC offers Bluetooth Low Energy support with an ARM® Cortex® M33F application processor, 256 KB RAM, 512 KB ROM, 1024-2048KB NVM, with ARM® TrustZone® enabled security features, and state-of-the-art power management to enable maximum lifetime in battery-operated devices.

This document describes how to implement hardware designs with the devices listed in Table 1-1. Table 1-1 also lists the EVKs applicable to this document.

EVK	SoC Package	SoC Part Number	Kit Part Number
Evaluation Kit for ATM5305 5x5 QFN	40-pin 5x5 mm QFN	ATM5305-3NC8QK	ATMEVK-5305-NQK-2
Evaluation Kit for ATM5305 4x4 BGA	93-ball 4x4 mm BGA	ATM5305-3NC8BV	ATMEVK-5305-YBV-2
Evaluation Kit for ATM5205 5x5 QFN	40-pin 5x5 mm QFN	ATM5205-3NC8QK	ATMEVK-5205-NQK-2
Evaluation Kit for ATM5205 4x4 BGA	93-ball 4x4 mm BGA	ATM5205-3NC8BV	ATMEVK-5205-YBV-2

Table 1-1 - ATM5/e Series EVKs

The following topics are covered:

- Migrating from Atmosic EVK to the final form factor design
- PMU Configurations
- I/O Connections
- Component Selection
- Layout Guidelines
- Matching Guidelines
- Production Test Guidelines

2. Migration Guidelines

2.1 Migrating from the Atmosic EVK to the final form factor design

The Atmosic EVK includes multiple connection options for demonstrating various PMU configurations, applications, and power consumption profiles. These options are not necessary for a final product form factor design. Follow these steps to complete your final form factor design:

1. Use the Atmosic EVK schematic and the guidelines in this document as a foundation for your final form factor design.
2. Be sure to reserve the necessary debug connector or test points for software development, firmware loading and debug message readout, based on the FW download protocol selected in the Signals and Timing for FW Download and Production Test section of this document.
3. Go over the checklist in the Guidelines and Checklist for Board Designs with ATM5/e Bluetooth SoC documentation

3. PMU Configuration

Please refer to the Supported PMU Configurations section of the **ATM5/e Series Reference Manual** for battery and I/O supply options. The following questions may help determine the correct configuration:

- What is the voltage range of the primary power source?
  - For voltages between 1.7 V and 3.3 V, VBAT3V must be used with the MODE pin tied to VBAT3V.
  - For voltages between 1.1 V - 1.6 V, VBAT1V must be used with the MODE pin tied to ground.
- Do on-board peripherals require an external I/O supply?
  - If the ATM5/e is interfacing to peripherals (e.g., Flash, sensors, etc), they must share an I/O supply. If a peripheral I/O supply needs to be greater than 1.8 V, an external I/O supply is needed.
  - The ATM5/e is able to power peripherals from its internally generated I/O supply up to an average of 30 mA (VBAT3V MODE).
    ***Note**: The ATM5/e PMU can sustain a maximum average load of 100 mW (measured at VBAT3V), which includes the ATM5/e as well as any peripherals that are being powered.*

4. I/O Connections

All of the ATM5/e digital I/O have programmable functionality, and it is recommended to use the Atmosic Pinmux Tool for selecting digital I/O functionality. Each digital I/O also has programmable drive strength and pull options. Please refer to the **ATM5/e Series Datasheet** for details. The following section covers some additional considerations:

- Power Down (PWD) should be pulled low to allow for debug and production test support. Pulses of voltage greater than 0.7 V and greater than 1 ms in duration are required when this pin is used for resetting the chip.
  - For applications where the primary power source can be disconnected or experience large voltage fluctuations for short periods of time, a PWD circuit (such as what is shown in Figure 4-1) is required to ensure the ATM5/e resets properly. The component values may need to be tuned to achieve the required pulse voltage and duration, depending on voltage

levels and ramp rate.

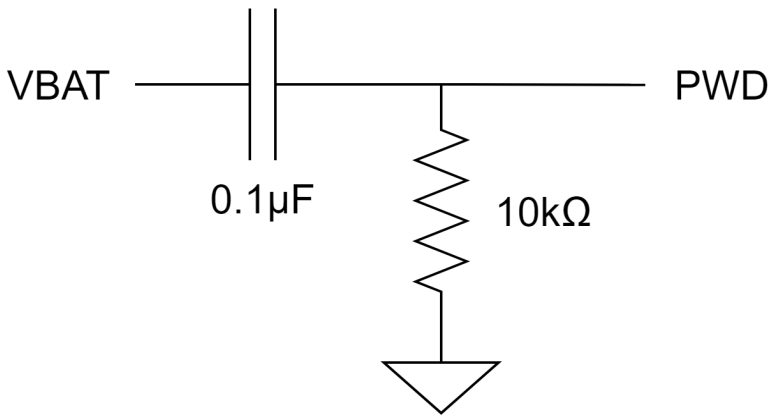


Figure 4-1 - Circuit to Generate PWD Pulse

- P25 should be pulled low to allow for debug and production test support. P25 must be low during software boot to allow for normal code execution. If P25 is high during software boot, the ATM5/e will enter an idle state suitable for certain operations such as programming or reading the on-chip NVM. After the software boots, P25 can be reconfigured and used as a normal GPIO. The size of the on-board pull-down resistor should account for any shared functionality. For example, an application that can reset while P25 is outputting high may need a stronger pull-down to ensure the pin is low during software boot after the reset.
- The default state for all ATM5/e digital I/O is high-Z with no internal pull-up or pull-down during Powerdown and SoC Off. In other power states, P0 and P1 default as inputs with an internal pull-down on P0 and an internal pull-up on P1.
- If an onboard resistor divider is connected to an Application ADC input, component values should not exceed 100 kΩ to avoid impacting measurement accuracy. Application ADC inputs should also be routed carefully to minimize noise coupling. Please refer to the **ATM5/e General Purpose ADC Application Note** for voltage ranges and configuration options. If a transistor is being used to enable the resistor divider (such as what is shown in Figure 4-2), the component values should account for the threshold voltage, and the Application ADC input should be pulled low when the transistor is off.

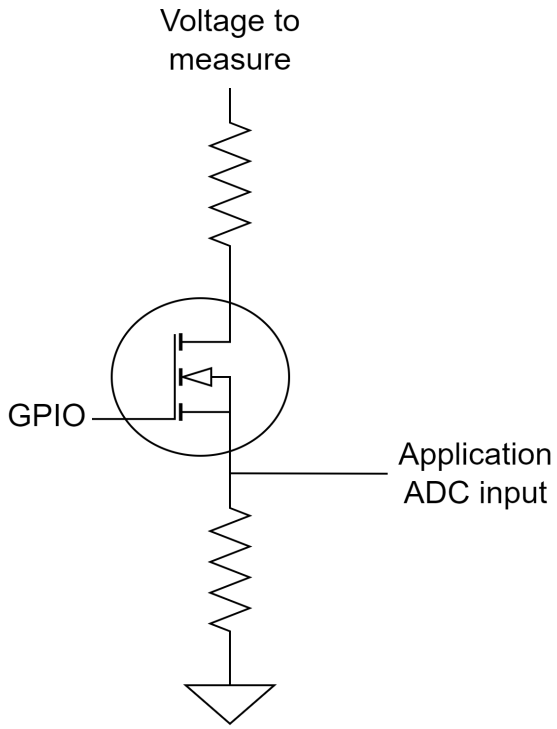


Figure 4-2 - Voltage Divider with a Transistor for Application ADC

- To support I2C clock stretching, software configures I2C_SCL as open-drain with internal pull-up by default, which may require an on-board pull-resistor depending on the I2C clock frequency.
- RES must be tied to ground.

5. Component Selection

5.1 32 MHz Crystal

The 32 MHz crystal used on the ATM5/e EVB is the ETSB32E00000ME from Hosonic (+/-8 ppm tolerance, +/-15 ppm stability, 9 pF load capacitance, 60 Ω maximum ESR).

This can be used as a reference when choosing alternate parts (e.g., Epson

FA-20H 32.00M-80AANNG50RE5 or ECS ECS-320-8-37B-CWN).

The ATM5/e supports up to +/-50 ppm total combined stability and tolerance as required by the Bluetooth specification.

The ATM5/e can support load capacitance up to 12 pF with internal tuning capacitors, but < 9 pF is recommended for lower power consumption.

If an alternate part with a different load capacitance is used, the ATM5/e internal tuning capacitors may need to be adjusted. This can typically be done via lab characterization:

1. Follow the instructions in the **Atmosic RF Test Tool User Guide** (available on the Atmosic Support website) to load the HCI vendor code to DUT, and install and run the Atmosic RF Test Tool.
2. Connect the DUT RF port to a spectrum analyzer.
3. Select the `CAL.` tab on the Atmosic RF Tool, and click the `Xtal Cal.` button. For each iteration, check the frequency offset on the spectrum analyzer, enter the value (Hz) in the pop-up window, and click Exit. Upon completion, the characterized value between 0 and 31 will be displayed in the Atmosic RF Tool.
4. Repeat step 3 on a handful of DUTs to confirm that the characterized value is similar across multiple devices.
5. Input the characterized value into the Atmosic Production Test Tool to be programmed during DUT manufacturing.

If a TCXO is used, its output needs to be positive (not going below 0V), and the peak-to-peak swing should be as large as possible, up to 1V max. The output should be connected to the XTALI_32M pin, and the XTALO_32M pin should be left floating. The Atmosic Production Test Tool should also be configured to program the device for TCXO operation.

5.2 32.768 kHz Crystal

The 32.768 kHz crystal used on the ATM5/e EVB is the SC20S-7PF20PPM from Seiko Instruments (+/-20 ppm tolerance, 7 pF load capacitance, 70 kΩ maximum ESR).

This can be used as a reference when choosing alternate parts (e.g., Micro Crystal AG CM8V-T1A-32.768KHZ-7PF-100PPM-TA-QC).

The ATM5/e supports up to +/-500 ppm total combined stability and tolerance as required by the Bluetooth 5.3 specification.

The ATM5/e can support load capacitance up to 12 pF with internal tuning capacitors, but < 9 pF is recommended for lower power consumption.

Care must be taken in assembly to avoid excessive solder flux that can create a parasitic impedance path between the two pins XTALI and XTALO. This parasitic PCB impedance must be more than 100Mohms, and the total impedance, combining PCB and the crystal and internal impedance of the chip, must not be less than 12Mohms.

If the application does not require a crystal, the XTALI_32k pin should be grounded, and the XTALO_32k pin should be left floating.

If the 32.768KHz clock requires trimming, please follow the clock trimming procedure below.

1. **Preparation:** Load the HCI_vendor code onto the device, install the Atmosic RF Test Tool, and launch the application as detailed in the *Atmosic RF Test Tool User Guide*.
2. **Calibration:**
    a. Navigate to the 32K Cal tab in the RF Test Tool.
    b. Select the appropriate GPIO to output the 32 kHz clock for measurement.
    c. Connect an oscilloscope to the selected GPIO pin.
    d. Adjust the XOCAP value within the tool until the output frequency measures exactly 32.768 kHz.
3. **Preparation for saving the setting**:
    a. Follow the instructions in the Atmosic MPTool User Guide Chapter 6 to install the MPTool software and the section 9.1.2 to enter the command line mode
4. **Issue the command to save the values**:
    a. `C:\AtmosicMP\bin>AtmMPTool.exe APT DISC`
    b. `C:\AtmosicMP\bin>AtmMPTool.exe APT 1 DUT SECJRNL DUMP origin_sec_jrnl.bin`
    c. `C:\AtmosicMP\bin>AtmMPTool.exe FILE NVDS origin_sec_jrnl.bin SHOW`
    d. `C:\AtmosicMP\bin>AtmMPTool.exe FILE LK_SECJRNL origin_sec_jrnl.bin TAG SET_32K_CAP_ATM5 “value” new_sec_jrnl.bin`
    e. `C:\AtmosicMP\bin>AtmMPTool.exe APT 1 DUT SECJRNL PUSH new_sec_jrnl.bin`
5. **Verification:** Power cycle the board and repeat the step 2 to verify if the frequency output on the oscilloscope is 32.768KHz

Example: Trimming the 32.768 kHz Clock

1. **Configure output**: In the 32K Cal tab of the RF Test Tool, select P8 as the GPIO pin to output the 32KHz clock.

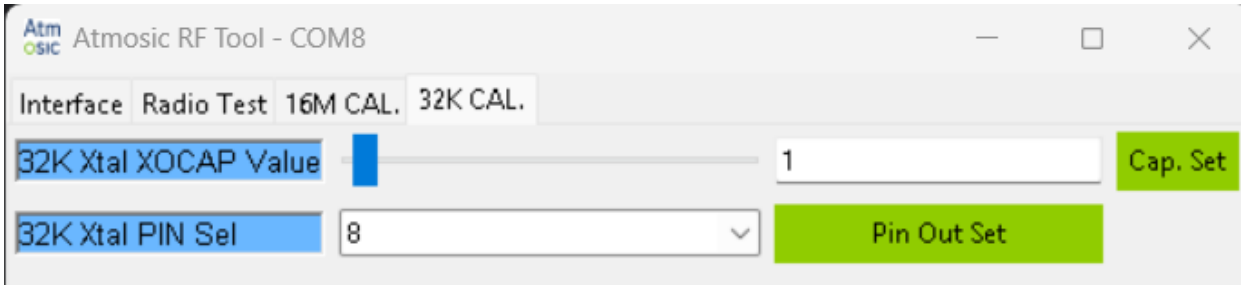


Figure 5-1 - RF Test Tool Configuration for 32K Crystal Calibration

2. **Measure:** Connect Oscilloscope to P8 (pin 9 on 60-pin header) .

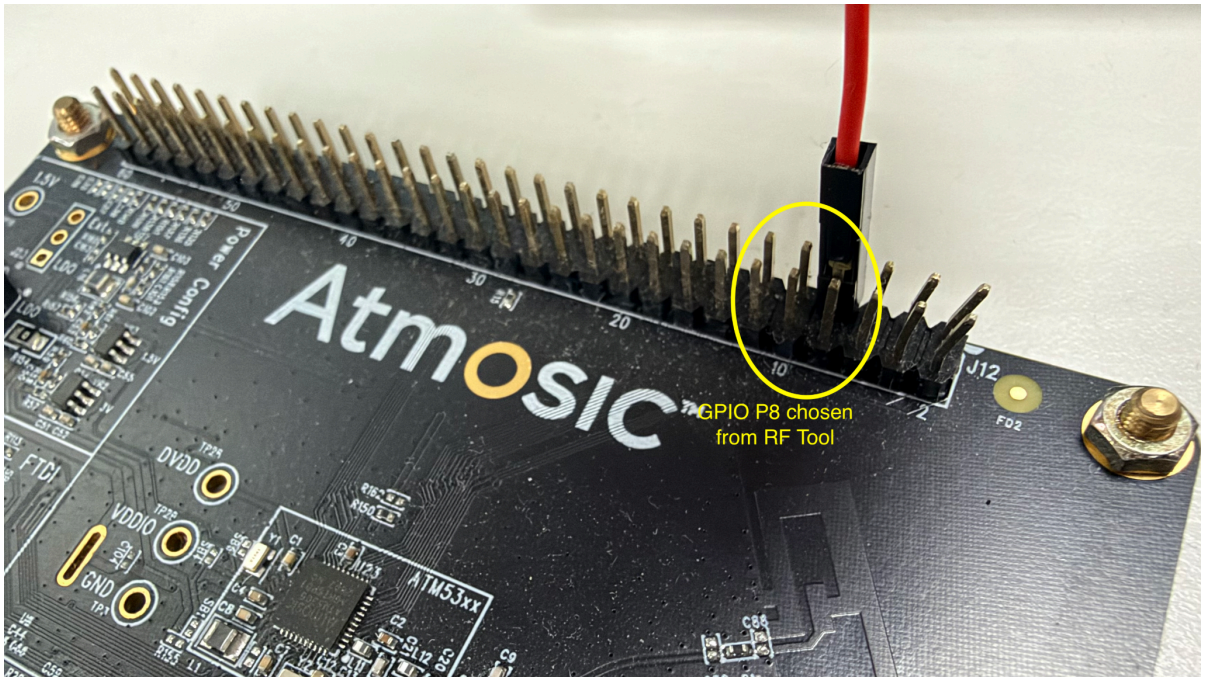


Figure 5-2 - Oscilloscope Connection in 32K Crystal Calibration

Use counter mode to measure the clock frequency. In this example, the frequency is 32.7623KHz before tuning.



Figure 5-3 - Clock Frequency Reading Before Calibration

3. **Calibration:** Adjust the XOCAP value in the tool and click Cap. set button to apply the new value until the frequency reaches 32.768KHz.

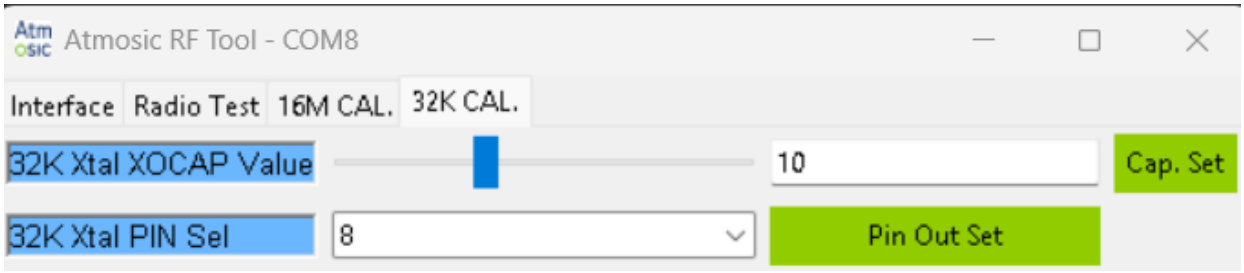


Figure 5-4 - Adjust XOCAP Value During Calibration

The frequency is now 32.7686KHz.



Figure 5-5 - Clock Frequency Reading After Calibration

4. **Save the setting**: Save the calibrated value to the chip using the MPTool command line mode (as detailed in step 4 of the Clock Trimming Procedure):
   a. `C:\AtmosicMP\bin>AtmMPTool.exe APT DISC`
   b. `C:\AtmosicMP\bin>AtmMPTool.exe APT 1 DUT SECJRNL DUMP origin_sec_jrnl.bin`
   c. `C:\AtmosicMP\bin>AtmMPTool.exe FILE NVDS origin_sec_jrnl.bin SHOW`
   d. `C:\AtmosicMP\bin>AtmMPTool.exe FILE LK_SECJRNL origin_sec_jrnl.bin TAG SET_32K_CAP_ATM5 19 new_sec_jrnl.bin`
   e. `C:\AtmosicMP\bin>AtmMPTool.exe APT 1 DUT SECJRNL PUSH new_sec_jrnl.bin`

5. **Verify:** Power cycle the board, reconnect the RF Test Tool, and re-enable the P8 output. The frequency on the oscilloscope should now be exactly 32.768 kHz, confirming the calibration value is successfully saved in the secure journal memory.

5.3 Switcher Inductor

The 2.2 µH multilayer chip power inductor used by the switcher on the ATM5/e EVB is the LQM2MPN2R2NG0L from Murata. The DC Resistance (DCR) of this inductor is

110/138 mΩ (typical/max), and the rated current is 1.2 A. If choosing an alternate part, it needs to have a similar DCR and a rated current of 600 mA or higher.

To prevent power inductor transient noise from coupling to the 2.4GHz RF antenna and degrading receive sensitivity, hardware designers must implement one of the placement and isolation rules outlined below.

1. place a ground shield trace between the antenna and the inductor
    - Trace width: <1mm
    - Add stitching vias and via pitch: <2mm (center to center gap)
2. separation between 2.4GHz antenna and inductor pad must be greater than 2.4GHz near field distance, 2 cm.

$$R < 0.62 \times \sqrt{\frac{D^3}{\lambda}} \approx 1.5\ \text{cm} \sim 2\ \text{cm}$$

5.4 Antenna Switch

If an antenna switch is necessary for Channel Sounding (CS) applications, the ATM5/e EVBs have been characterized with the Murata XMSSJR8G2PA-246 to work well for all channel sounding performance metrics down to T_SW=2 µs (CS antenna switch time). If a different antenna switch is desired, then the following guidelines should be met:

1. The switching time specification is usually defined as a change of amplitude power (say to 10% or 90%) and not how long it takes for an RF carrier tone's phase to settle after switching antenna ports. For a given CS switching time specification (1, 2, 4, or 10 µs), make sure the switching time is sufficiently fast to allow for the phase to settle, such as by measuring the CS phi_zmd specification.
2. 30 dB or higher port isolation.

6. Layout Guidelines

This section describes layout guidelines to be followed on some key signals/routes to/from the ATM5/e.

6.1 RFIO Section

The ATM5/e EVBs have a matching circuit as shown in Figure 6-1 and component values in Table 6-1.

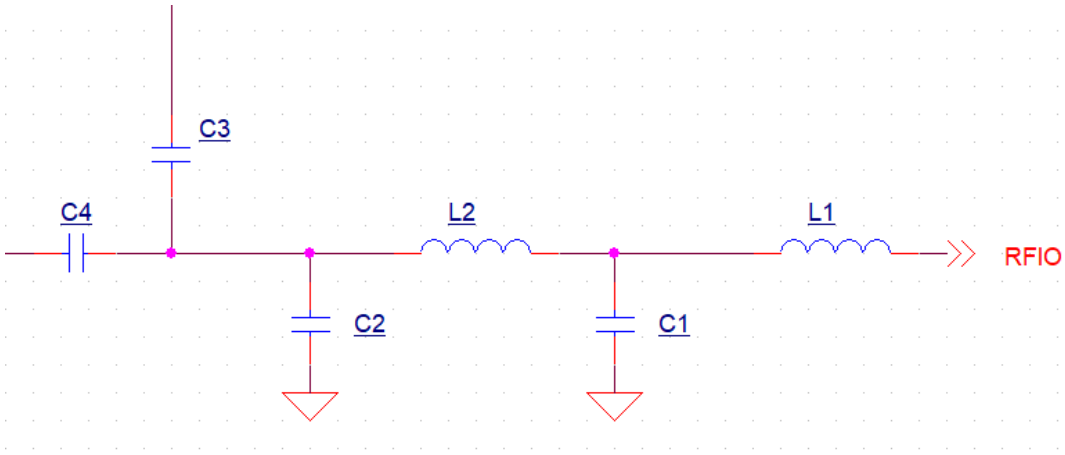


Figure 6-1 - RFIO Matching Circuit

EVB	Part Reference in Figure 3	Part Reference in EVB	Value
ATM5/e EVB	L1	L11	3.0 nH
	C1	C21	1.5 pF
	L2	L12	2.7 nH
	C2	C20	1.0 pF
	C3	C65	27 pF
	C4	C86	DNS

Table 6-1 - RFIO Matching Circuit

The two series inductors (L1 and L2) and two shunt capacitors (C1 and C2) function as a low-pass filter (assuming a pure 50 Ω termination at all harmonic frequencies) to reject higher harmonic frequencies to meet FCC requirements. To maximize harmonic rejection and minimize fundamental power loss, it is recommended that type MHQ series inductors from TDK or LQP03HQ series inductors from Murata be used. If an antenna with good inherent harmonic rejection is used, this filtering network may be simplified. L1 value may be increased slightly to 3.3nH or higher for the smaller BGA

package to compensate for the smaller internal series inductance on the RFIO pin of the package.

The series 27 pF capacitor functions as a DC block and can be placed at C3 or C4, depending on whether the RF signal is connected to J4 for conducted measurements or to the RF Switch U1 for over-the-air measurements using the on-board antennas. It is strongly recommended to add an ESD protection device at the antenna if the antenna is exposed to external physical contact either during assembly or in the final product and does not provide a low-impedance path to GND. If a PIFA, which has a DC short to GND, is used, an ESD protection device is not needed. Such an antenna is recommended.

An example of such a device is the ESD150-B1-W0201 from Infineon, which can significantly boost the ESD voltage protection beyond the industry standard requirement met by the ATM5/e. This optional extra protection may be used when the board is assembled in an environment where the ESD voltage exceeds that allowed by industry standards. An alternative device with comparable specifications to the ESD150-B1-W0201, especially the clamping voltage and line capacitance, may be used.

As for the placement of these components on the PCB, it is critical that the 4 lowpass filter components (L1, C1, L2, C2) be placed next to each other and as close to the ATM5/e as SMT assembly allows, minimizing any parasitic inductance resulting from the connecting trace, to maximize the effectiveness of the filtering and matching. It is also recommended that C1 and C2 are physically separated and not share a GND via.

Furthermore, the current selection of the values of the filter and matching components listed in Table 6-1 above assumes the fixed distance between L1 and the ATM5/e on the EVB. In a layout where this distance is different, the values of the filter and matching components will need to be adjusted accordingly. L1 and C1 will be the most likely components to be adjusted to compensate for that distance.

The layout of the EVB PCB has this transmission line modeled as a Coplanar Waveguide (CPW) with a characteristic impedance of 50 Ω. The trace width/spacing can be adjusted according to the board stack-up.

If additional tuning is required, please note that the impedance of the match discussed in Table 6-1 when looking out from the RFIO port (using a pigtail placed at the RFIO pin, without the ATM5/e), towards the match is roughly 40+j35 at 2.44 GHz and 6+j80 at 4.88 GHz. This is the load impedance of the ATM5/e PA that will ensure the optimum transmit power, efficiency, and harmonics. This same load will, at the same time, ensure a good match for the receiver.

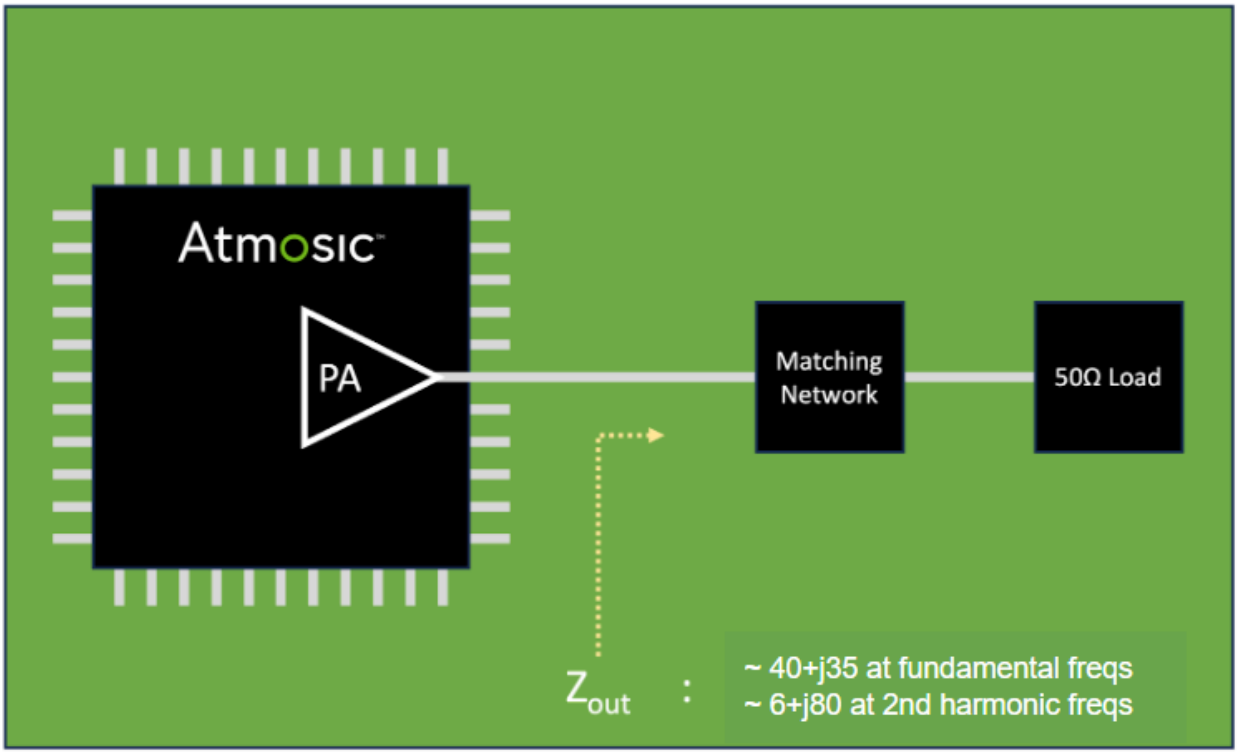


Figure 6-2 - RFIO Match Circuit Block Diagram

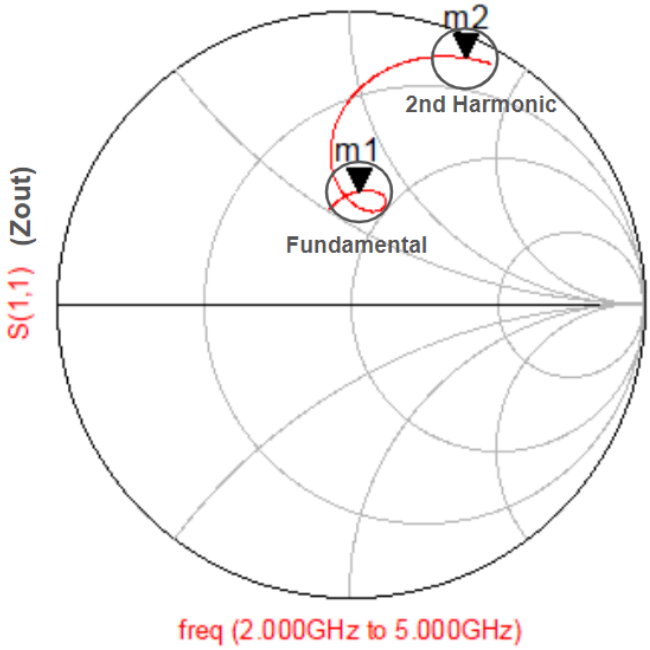


Figure 6-3 - Simulated RFIO Match S11 Looking Out from the SoC

6.2 Board Stack-up

While the board stack-up can be chosen according to the needs of the application, the stack-up of the current version of ATM5/e 5x5 QFN EVBs is shown below. The board thickness is 62 mils (or 1.58 mm).

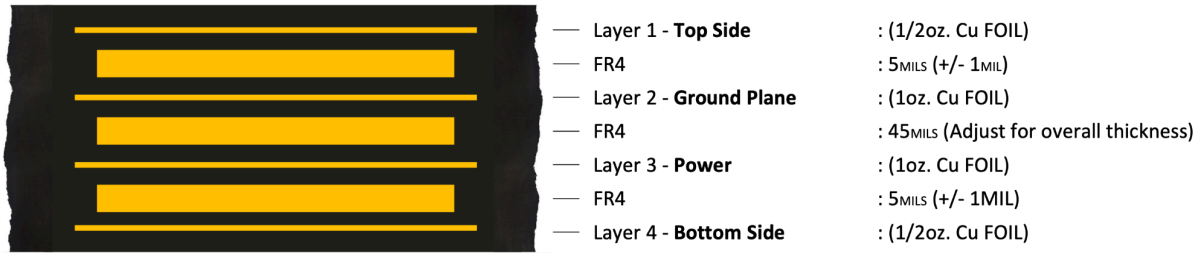


Figure 6-4 - Board Stack-Up

Also, shown below is an alternative example of a 4-layer stack-up for thinner (32 mils/0.8 mm) PCBs.

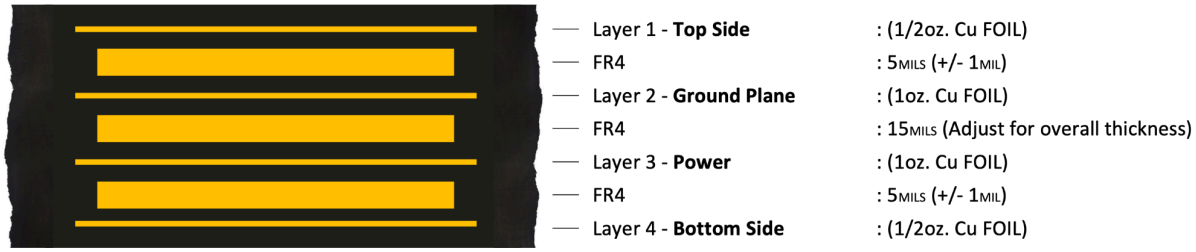


Figure 6-5 - 4-Layer Stack-up for Thinner PCB

And shown below is the stack-up of the current version of the EVB based on the ATM5/e in a BGA package. The total thickness of this EVB is 61.3 mils. Six layers are needed to allow access to the inner-row pins without perforating the GND plane underneath the chip and using costly via-in-pad technology. This can be accomplished by routing the inner-row pins on Layer 2 through blind vias placed in the free space between the inner row and the center GND pins. Layers 3 and 5 are used as GND planes. Layers 4 and 6 can be used for routing.

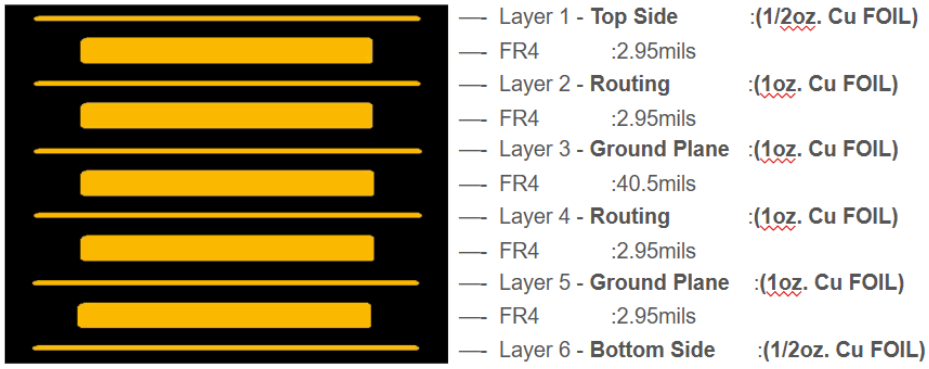


Figure 6-6 - 6-Layer Stack-up for ATM5/e BGA EVB

6.4 Switcher Inductor

For ATM5/e 5x5 QFN-based 4-layer PCBs, the 2.2 µH switcher inductor needs to be placed as close as possible to pins 30 and 31. However, priority is given to the decoupling capacitor connected to pin 31 (VBAT1V), pin 29 (VBAT3V), and pin 28 (VDDIO). A trace width of at least 10 mils is recommended to minimize trace resistance, and the loop area formed by the traces, inductor, and the Atmosic device should be minimized. Avoid routing sensitive small analog signals on all layers beneath the inductor. Figure 6-7 below illustrates a recommended layout for the above-mentioned guideline.

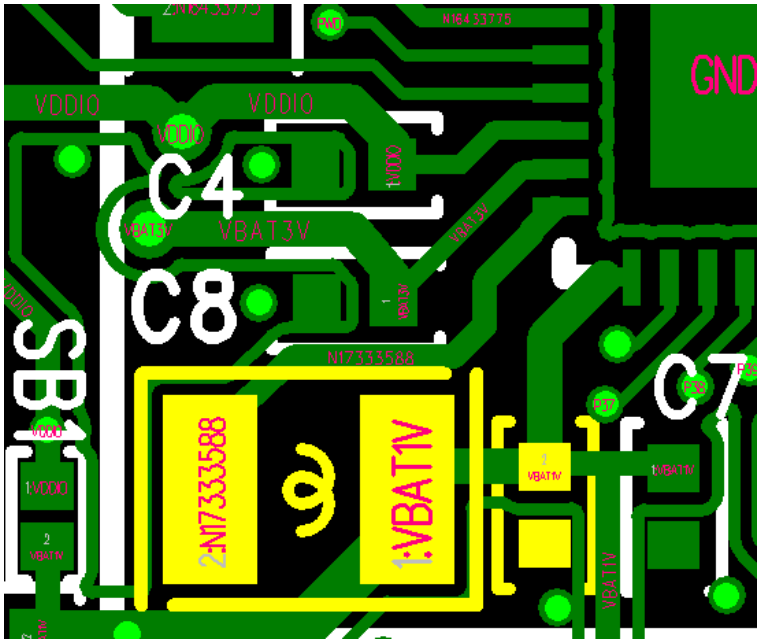


Figure 6-7 - Switcher Inductor Layout Recommendation for ATM5/e 5x5 QFN-based PCB

For ATM5/e BGA-based 6-layer PCBs, the recommendation is also similar to the 5x5 QFN package, but its respective pins are different for the inductor and nearby voltage rails: pins A11 and C11 for the inductor, and bypass capacitors close to pin L5 (VBAT3V), pin L8 (VDDIO), and pin A11 (VBAT1V).

6.5 Connecting VBAT1V to VBAT1V_A

The placement of bypass capacitors on the analog rail and their routing from the VBAT1Vpin to the VBAT1V_A pin is critical to the performance of the radio block:

- Place the 10 µF bypass cap on VBAT1Vas close as possible to the pin (pin 31 on PCBs with 5x5 mm QFN package, , or pin A11 on ATM5/e with 4x4 mm BGA package). This capacitor must be placed on the same layer as the ATM5/e device.
- While routing VBAT1V to VBAT1V_A via the RC filter, place the via closer to the VBAT1V bypass capacitor than to the pin/pad itself. In doing so, the VBAT1V pin “sees” less inductance (thus lower impedance) to the bypass capacitor than to the remaining trace.
- Place the RC filter (1 Ω + 20 µF) close to the VBAT1V_Apin to filter out effectively any noise that may get on the VBAT1V supply trace. The two 10 uF capacitors can be combined into one 22 uF for PCB space saving or cost

saving. The VBAT1V supply level should be within +/- 5% for performance and +/- 20% for functionality.

7. Production Test Guidelines

7.1 Signals and Timing for FW Download

The ATM5/e series supports SWD interface for firmware download. The SWD signal test points must be reserved for development and production purposes

Signals for the SWD interface are:

1. GND
2. VBAT3V or VBAT for powering the DUT
3. PWD to reset DUT for entering the FW download mode (Benign Boot mode)
4. P25 to select boot modes, P25 = VDDIO (High) = BBOOT mode, P25 = Ground (Low) = Normal boot, Selected during the SoC power up process
5. P0 for SWDCLK, P1 for SWDIO to program the DUT

SWD signal timing sequence:

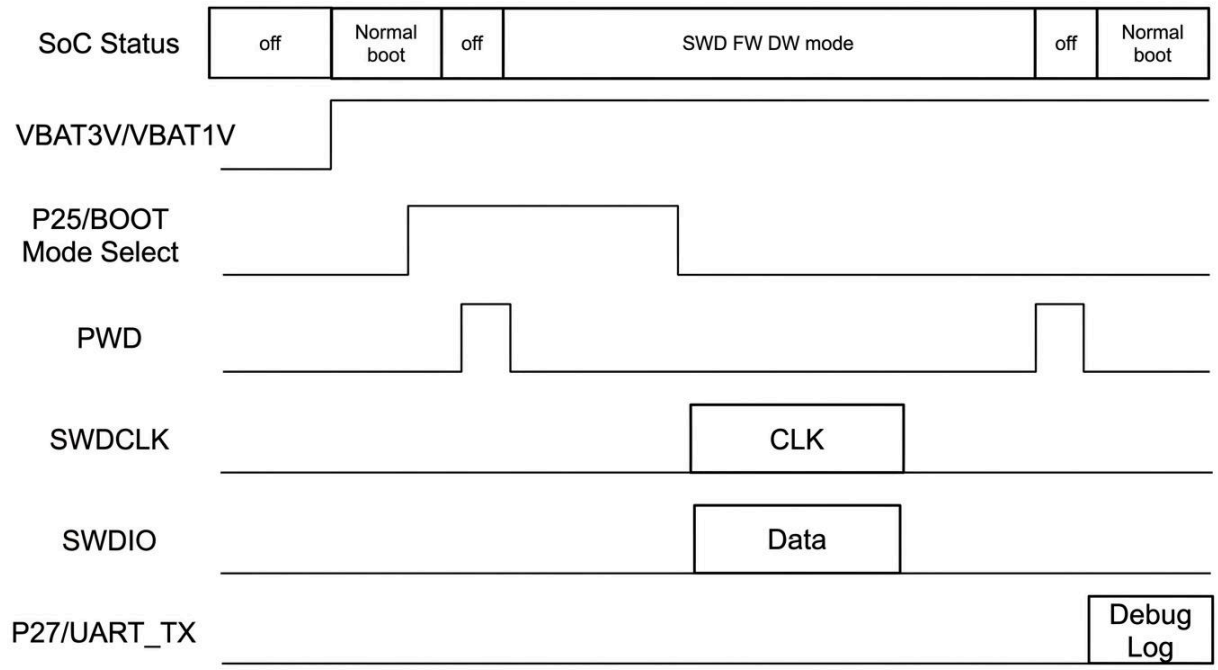


Figure 7-1 - SWD signal timing sequence

The Atmosic firmware download driver in the ROM Bootloader Host, or MPTool handles the timing of the signals. From a hardware design perspective, pogo pin probing points or a debug connector must be reserved if the SWD programming interface is used for mass production.

7.2 Production and Certification Test

Signals for HCI RF testing are:

1. GND
2. VBAT3V or VBAT1V for powering the DUT
3. PWD to reset DUT from any unknown status
4. UART0_TX, UART0_RX, UART0_RTS, UART0_CTS

UART0 for RF testing supports DTM (2-wire) and HCI (2-wire or 4-wire) protocols. Atmosic EVK and SDK select P29 for UART0_TX, P28 for UART0_RX, P17 for UART0_RTS and P30 for UART0_CTS. Referring to the Atmosic Pinmux Tool for other available IO pins. UART0_CTS and UART0_RTS can be omitted if the flow control is not required.

7.3 Programming OTP

The following OTP fields need to be programmed based on the security requirements:

- uart1_rx_disable
- sec_dbg_config

Please refer to the OTP Memory section of the **ATM5/e Series Reference Manual** for details regarding these fields.

Reference Documents

Title	Document Number
ATM5/e Series Datasheet	6494-xxxx-xxxx
ATM5/e Series Reference Manual	10048-xxxx-xxxx
Atmosic RF Test Tool User Guide	ATM-UGRF-xxxx

Revision History

Date	Version	Description
November 2, 2026	0.10	Initial version created.

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