ATM2202

Extreme Low Power Bluetooth 5.0 SoC with Embedded Flash

Atmosic™

Datasheet

Overview

The ATM2202 is part of a family of extreme low-power Bluetooth® 5 system-on-a-chip (SoC) solutions. This Bluetooth Low Energy SoC integrates a Bluetooth 5.0 compliant radio with ARM® Cortex® M0 application processor, 1 MB embedded Flash, 128 KB Random Access Memory (RAM), 256 KB Read Only Memory (ROM), 4 KB One-Time-Programmable (OTP) memory, and state-of-the-art power management.

The extremely low power ATM2202 SoC with 1 mA active Rx and 2.5 mA active Tx is designed to extend battery life for the Internet-of-Things (IoT). Support for low duty cycle operation allows systems to run for significantly longer time periods without battery replacement.

The ATM2202 is available in a 40-pin 5 mm x 5 mm QFN package.

Applications

Industrial and Enterprise
- Beacons and Sensors
- Asset Tracking
- Environmental Monitors

Healthcare
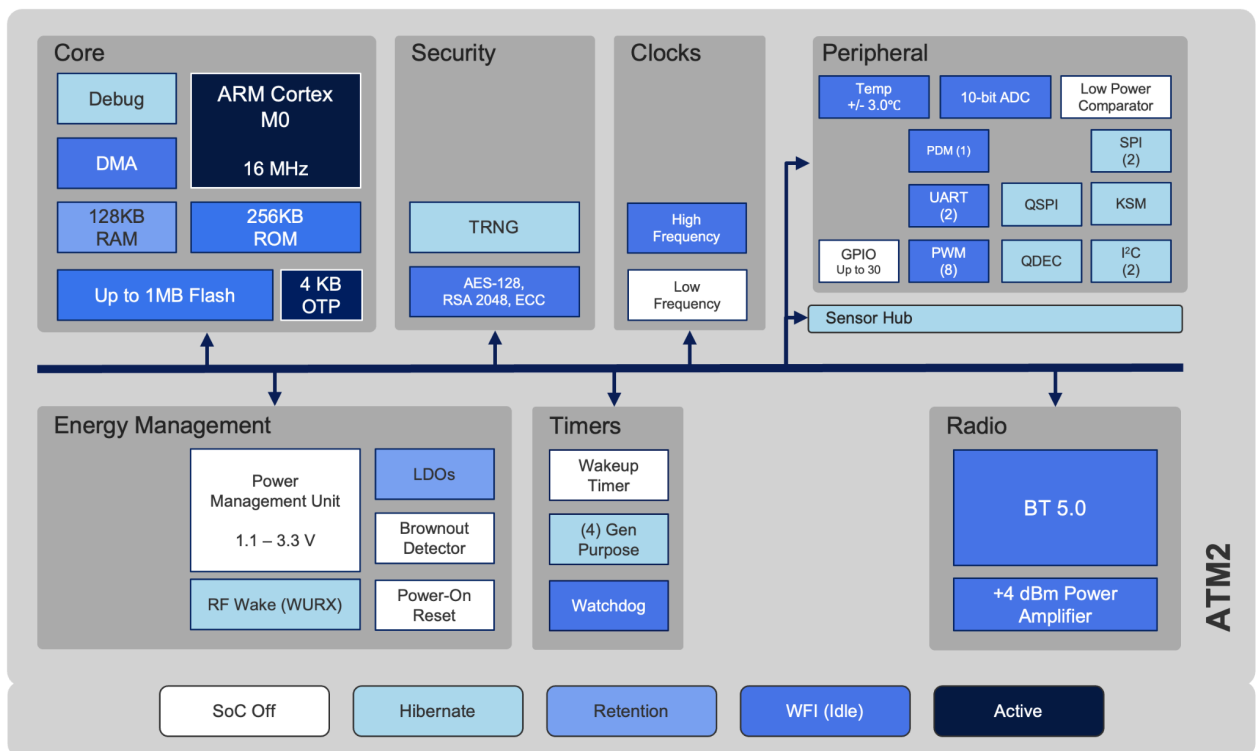- Thermometers
- Asset Trackers
- Patient Monitoring

Home
- Home Automation
- Remote Control
- Human Interface Devices (HID)

Personal
- Wearables

Auto
- Key fobs and Accessories

Features

- Compliant with Bluetooth 5.0 standard
- Supports Bluetooth 2 Mbps, 1 Mbps, 500 kbps, and 125 kbps
- Fully integrated RF front-end
- SoC typical power consumption with 3 V battery including PMU
    - **Active Rx @ -95 dBm: 1.0 mA**
    - **Active Tx @ 0 dBm: 2.5 mA**
    - **Retention @ 32 KB RAM: 2 µA**
    - **Hibernation with Wakeup Receiver: 0.95 µA**
    - **Hibernate: 0.8 µA**
    - **Soc Off: 300 nA**
- CPU: 16 MHz ARM Cortex M0 processor, programmable interrupt router
- Memory: 1 MB embedded Flash, 256 KB ROM, 128 KB RAM, and 4 KB OTP

- Retention RAM configuration: 16 KB to 128 KB in 16 KB step sizes
- RF Wakeup Receiver
- Interfaces: I2C, SPI, UART, PWM, GPIO
- 10-bit application ADC
- Digital microphone Input (PDM)
- SWD for interactive debugging
- AES-128 hardware
- True random number generator (TRNG)
- Sensor Hub
- Keyboard Matrix Controller (KSM)
- Quadrature Decoder for mouse input (QDEC)
- 16 MHz / optional 32.768 kHz crystal oscillator
- 1.1 V to 3.3 V battery input voltage with integrated Power Management Unit (PMU)
- Package: 40-pin 5 mm x 5 mm QFN

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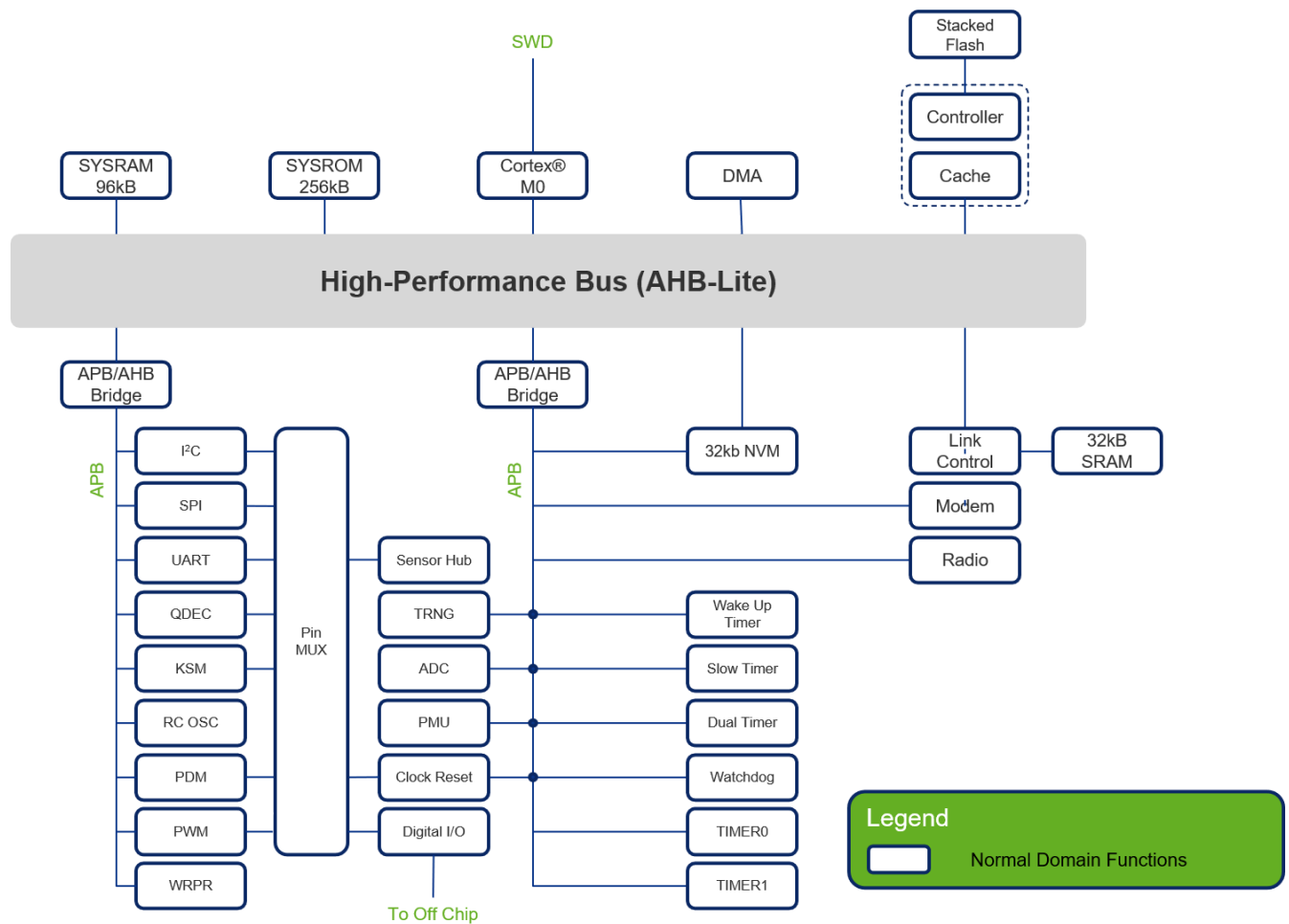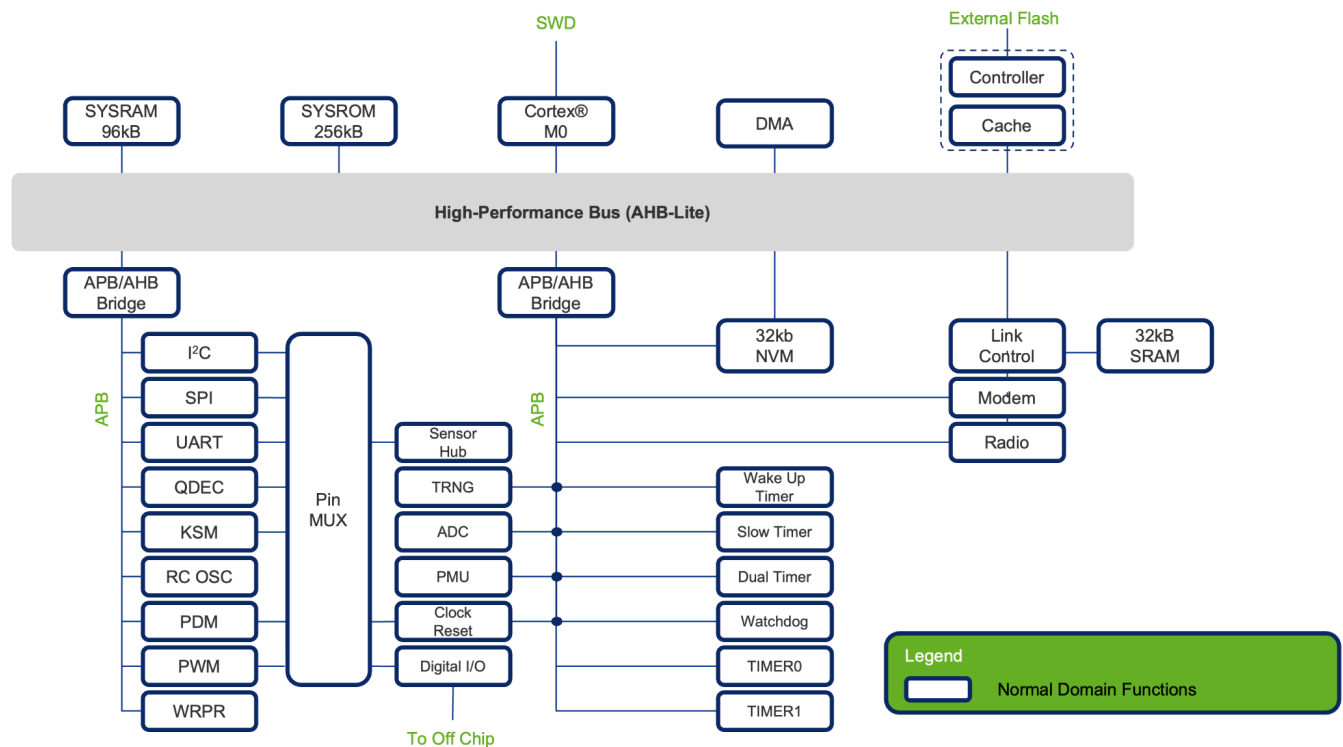
1.1 CPU & Memory

The ATM2202 contains a 16 MHz 32-bit ARM® Cortex®-M0 processor that is optimized for low-power operation. The processor is a little endian, 32-bit RISC processor which implements the ARMv6-M architecture specification. It supports most Thumb-1 instructions and some Thumb-2 instructions. It features four breakpoints, a serial access debug port, 32 interrupts, a single cycle multiplier, full wake-on-interrupt support, and two watch points.

To reduce latency, software can use the Direct Memory Access (DMA) core for memory to memory copying and for initializing blocks of memory to a constant. When it is in use, the DMA core masters the Advanced Microcontroller Bus Architecture (AMBA) High-performance Bus (AHB) and has higher precedence than the Cortex®-M0.

The ATM2202 includes the following memory components:

- ROM: 256 KB of ROM containing the Bluetooth LE 5 protocol stack up to GATT/GAP layer, a beacon application, and the boot code
- SRAM: 128 KB of SRAM containing both system RAM and data RAM organized as eight 16 KB macros. Two of the macros are reserved for the Bluetooth 5 link controller. The power state of each macro in each low power state can be independently controlled
- NVM: 4 KB of One-Time-Programmable memory (OTP) to store configuration, calibration data, and user data
- FLASH: 1 MB embedded flash for customer applications.

There is one quad SPI (QSPI) master port connected to the embedded flash and supports up to 32 MHz.
Internally there are three cores that can act as master for the interface:
(a) 1-bit core identical to the SPI core described in the Peripherals and I/O section. It provides read and write support to

the embedded flash via indirect addressing.

(b) Software specified protocol / content. The hardware's role is limited to serial shift in or out. Read and write access via indirect addressing is provided by this core.

(c) Direct memory mapping of the entire embedded flash contents. It essentially acts as an AHB bridge to the embedded flash. The hardware handles all protocols. Additionally, this core contains a cache in the read direction to reduce latency.

The quad SPI master port is equipped with a cache in the read direction to reduce the effective latency of flash accesses. Performance operating out of flash is comparable to that of operating out of RAM. When executing out of RAM and at 16 MHz, the ATM2202 has a CoreMark 1.0 score of 29.5. When executing out of embedded flash, with the quad SPI interface boosted to 32 MHz, the quad SPI cache enabled, and the remainder of the SoC operating at 16 MHz, the ATM2202 has a CoreMark 1.0 score of 25.7. Pins P1 and P2 can be used to access the Cortex®-M0's serial wire debug (SWD) port. The on-chip system memory is organized as follows:

Table 1.1-1   System Memory Map

Start	Stop	Block
0x0000 0000	0x0003 FFFF	ROM
0x1000 0000	0x100F FFFF	FLASH
0x2000 0000	0x2001 7FFF	SRAM
0x3000 0000	0x3000 FFFF	Link Controller
0x4000 0000	0x4000 FFFF	APB0_Peripherals
0x4001 0000	0x4001 1FFF	GPIO
0x4001 F000	0x4001 FFFF	SYSCTL
0x5000 0000	0x5000 FFFF	APB1_Peripherals
0x6000 0000	0x6000 0FFF	NVM
0x7000 0000	0x7000 0FFF	DMA
0x8000 0000	0x8000 0FFF	PDM

1.1.1 Clocks

There are three primary clock domains on the ATM2202:

- low power clock: 32.768 kHz crystal or an internal RC oscillator (RCOSC)
- medium power clock: 16 MHz crystal or an internal RC oscillator (RCOSC)
- high power clock: used by quad SPI for embedded flash

1.1.2 Reset

The PMU releases the chip-wide reset once the power supplies have stabilized. There is no explicit reset pin on the ATM2202 but the user can use PWD for an equivalent purpose. Many of the internal modules can additionally be reset through a software register write.

1.1.3 Power Modes

The SoC supports five primary power states which are Active, Retention, Hibernation, SoC Off, and Powerdown. Each primary state may have several secondary states depending on the number of active power domains and clock gating.

1. Active: All regions of the SoC are powered on. Active power can be optimized by utilizing clock gating registers and/or by putting the Cortex-M0 into Wait for Interrupt (WFI).
    - CPU Idle: When the CPU function is not required, it can be placed into WFI state to conserve power.
    - Bluetooth LE Deep Sleep: Bluetooth subsystem is powered down while the remainder of the ATM2202 is powered up. This state is useful when data needs to be processed but does not need to be transmitted over RF.
2. Retention: All or some of the 128 kB SRAM, in increments of 16 kB, can be retained. All register/flip-flop states are retained. Digital I/O's will hold the state they were at when the transition into either Hibernate or Retain started. Wake can be from a timer expiring, activity detected on GPIO's, activity detected on the keyboard, activity detected on the mouse, the sensor hub reading measurements crossing a threshold, and the detection of a connection over the SWD interface. All selections about how to wake need to be programmed before the transition into the low power state is triggered. The SRAM supply voltage can be lowered to further reduce leakage power consumption.
3. Hibernation: Powers down system memory. Retains only a minimal amount of flip-flop state. Retains I/O state. Wake up setting must be programmed before transitioning into this state.
4. SoC Off: all digital domains including the top level digital domain are powered down, but the PMU remains on in an ultra low-power state with limited functionality. The system must do a complete, cold start reboot when returning from this state to an active state. Wake mechanisms are limited to (a) special 40-bit timer, (b) external digital input on P10, (c) ultra-low power analog comparator with input on P11.
5. Powerdown[1] (PWD pin asserted): All power domains including the PMU are completely shut off. No supplies are internally generated or maintained. This state is only valid with an external I/O supply.

1.2 Security

The ATM2202 has a true random number generator (TRNG) which generates a single 32 bit random number per invocation. Arbitrarily long random numbers can be achieved by repeatedly invoking this random number generator. The outputs of TRNG can be used to generate public and private keys which in turn can be used to generate the link layer symmetrical key.

The ATM2202 also has an AES-128 hardware accelerator. This core is directly accessible by software and it is also used by the hardware to encrypt and decrypt packets when needed during Bluetooth LE operation.

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[1] Minimum PWD assertion time is 100 μs.

If necessary a fuse within the OTP can be set to disable all slave interfaces. This would prevent keys being read out by a third party but it would also disable the SWD interface which in turn blocks future debug. Setting this disabling fuse should be used with caution. Alternatively, writing to the OTP can be permanently blocked. This mechanism would prevent the alteration of public keys but would not block the SWD interface.

1.3   Power Management

The power management unit provides the core and I/O power supplies to the ATM2202 SoC. PMU generates the three power supply outputs: DVDD1P, AVDD1P, VDDIOP, and a fourth auxiliary supply VAUX used internally by the PMU. The following connections must be made on the board:
- DVDD1P to DVDD1
- AVDD1P to VDD1A

Table 1.3-1   PMU External Pins

PIN	Description
VBAT	Battery input. Battery voltages from 1.1 V to 3.3 V can be used. Must be connected to a battery or external supply.
LEXT1, LEXT2	Terminals between which the switching regulator inductor is connected.
DVDD1P, AVDD1P VDDIOP	DVDD1P and AVDD1P are PMU generated digital and analog core supply outputs. VDDIOP is a PMU generated 1.8 V I/O supply output.
VAUX	Auxiliary supply output of typical value 3.2 V, used internally by the PMU.
DVDD1, VDD1A	Power supply input for digital and analog core circuits.
VDDIO, VDDIOA	Power supply input for digital and analog I/O circuits.

The PMU provides multiple brownout interrupts to enable more reliable operation.

1.3.1 PMU Configurations

The PMU must be configured correctly to ensure correct operation. The following modes of operation are supported by the PMU:

(a) One external power supply or battery with external I/O supply:

For applications that cannot support fixed 1.8 V I/O supply
- Connect VBAT to VDDIO/VDDIOA
- Connect VAUX to VDDIOP
- Disable IO supply generation

(b) One external power supply or battery with internally generated I/O supply:

For applications that can use a fixed 1.8 V I/O supply for better power consumption or VBAT <= 1.8 V
- Connect VDDIOP to VDDIO/VDDIOA

## 1.4   Sensor Hub

The sensor hub is a hardware module that, when suitably programmed, can read data from external sensors and write to embedded flash on the quad SPI interface. This function can be performed with all other power domains, including the CPU power domain, powered down. Additionally, the sensor hub can trigger a chip wide wake up if any of the read data crosses preprogrammed thresholds.

1.5 Bluetooth LE Radio

The block diagram of the low-power radio is shown in Figure 1.5-1. The radio supports Bluetooth 5.0 including 1 Mbps basic PHY, 2 Mbps high-speed PHY, 500 kbps, and 125 kbps PHY. The basic 1 Mbps PHY is compatible with Bluetooth 4.0, while the 2 Mbps rate provides 2X speed and the long range rates provide up to 4X range. The transmit path uses digital direct frequency modulation of a fractional-N synthesizer to create a constant amplitude GFSK signal that is amplified by a power amplifier to provide the desired RF output level. On the receive path, an incoming RF signal is first amplified by an LNA before downconversion to baseband and digitized by two successive-approximation analog-to-digital converters. The digitized signal is sent to the Modem for further digital processing. The radio architecture is optimized for burst data transmission using Frequency-Hopping Spread Spectrum (FHSS) with 40 channels with 2 MHz spacing (3 advertising channels/37 data channels). Only a single RF Input/Output pin is needed, thereby simplifying board-level design.

Figure 1.5-1　　　　　　　　**Bluetooth LE Radio Block Diagram**
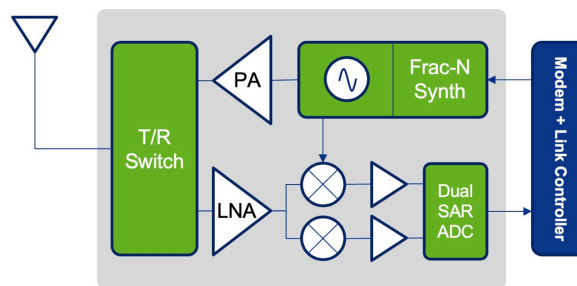

1.5.1 Link Controller

The Bluetooth 5 link controller (LC) and host stack provides an interface between the microcontroller (MCU), modem (MDM) and exchange memory (EM), allowing the MCU to access through the AHB bus to the control registers and exchange memory.   During transmission, software writes the packet payload and control structures into the exchange memory. The link controller serializes the data into a bit stream to the modem.   During receive, the operation is reversed. Received data from the modem is processed and stored in the exchange memory to be read by software. The design runs on an 8 MHz clock and is synchronous to MDM (16 MHz) and AHB bus (16 MHz) and exchange memory (16 MHz).

1.5.2 Modem

The modem (MDM), along with the radio, link controller, and software stack, forms a highly efficient Bluetooth 5 solution. Transmission and reception at rates of 2 Mbps, 1 Mbps, 500 kbps, and 125 kbps are supported.   During receive operation, the modem and radio are enabled prior to expected packet reception as determined by the link controller. Incoming packets are detected, tracked, processed, and then forwarded to the link controller. The modem and radio receiver are turned off by the link controller at the end of a completed packet. Channel information is provided directly from the link controller to the radio without involvement of the modem. There is minimal involvement of the modem in the transmit process. The link controller provides the symbol bit stream, which is then shaped consistent with the GFSK requirements to provide a frequency deviation for the radio. Channel information and target transmit power are provided directly from the link controller to the radio.

1.6   Wakeup Receiver

Figure 1.6-1   **Wakeup Receiver Block Diagram**
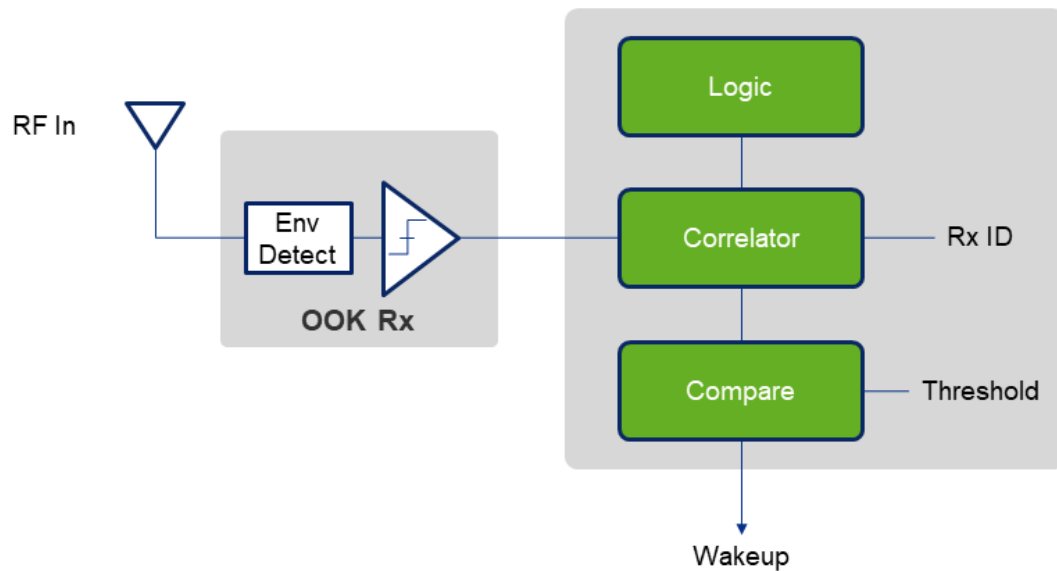
The use of a wakeup receiver allows a system to be in sleep mode while waiting for incoming RF activities. In this SoC, the wakeup receiver is designed to decode an incoming RF paging or wakeup signal with very low power consumption. This dedicated low-power wakeup receiver continuously monitors the incoming RF signal for a predefined paging signal. This continuous Rx mode is based on an OOK radio, which has ultra-low power consumption. The wakeup receiver is intended for short range and short latency applications. Latency of the wakeup receiver is typically in the order of 20 ms to 1 s, depending on the length of the Rx ID code used to identify the target device.

1.7 OTP Access

The OTP is accessible through two separate cores. One resides on the Advanced Peripheral Bus (APB) and provides indirect access for byte reads and bit writes. The other resides on the AHB bus and provides memory mapped addresses for byte, half word, and word reads.

1.8 Timers and Interrupts

1.8.1 Wakeup Timer

Wakeup timer is a 40-bit timer based on the low power 32 kHz clock. When this timer is enabled during SoC Off mode, it will determine the SoC Off duration.

1.8.2 General Purpose Timers

There are four general purpose timer cores: Timer0, Timer1, Dual Timer, and Slow Timer. The value of the timers are readable by the CPU. All timers are clocked by the medium power clock except for the Slow Timer which uses the low power clock. All these timers stop when the system enters a low power mode. The state of the timer is maintained during Retention mode but is reset during hibernate mode.

- Timer0, if enabled, will decrement from a 32 bit reload value to 0 triggering a maskable interrupt as it transitions from 1 to 0. The reload value is loaded as the next timer value when the timer reaches 0.
- Timer1 is identical to Timer0.
- Dual Timer contains two timers and each timer is independent of the other but sharing a single interrupt output. Each timer counts down and can run in one-shot, periodic, or free running mode. The timers are configurable to be either 16 bit or 32 bit. Additionally there is a rescale in front of each timer that can reduce the incoming clock by 1x (no change), 16x, or 256x.
- Slow Timer is a 40-bit count down timer with three programmable thresholds. The interrupt is optionally asserted when the counter counts from one above the threshold to the threshold. It is recommended that the timer be read twice and the value used only if the values from both reads are the same. If the values are not the same then the read should happen a third time. The timer is updating every 16000000/32768 cycles or approximately 488 cycles of the 16 MHz medium power clock.

1.8.3 Interrupts

There is one non-maskable interrupt and it is the watchdog interrupt. There are 32 possible maskable interrupts of which 16 are connected to the GPIO interrupts and 16 are the programmable combination of 48 possible interrupt sources. Each of these 16 configurable interrupts has its own combining function.

1.9 Pin Multiplexing

The ATM2202 supports 12 programmable pins. In addition, each of these I/O pins can be configured to be input only, output only, input/output, with or without pull-up.

1.10 Peripherals and I/O

The following peripherals are supported by the SoC.

- **GPIO**
  There are up to 12 GPIOs in the ATM2202. In addition to providing general purpose read and write access, the GPIO can also be used to generate interrupts and to wake the ATM2202 from low power states.

- **I2C**
  There are two identical I2C masters. Software preloads the transaction and then initiates the hardware controller. Software can either poll for completion or respond to the completion interrupt. I2C clock speed is programmable and ranges from 3.9 kHz to 4 MHz.

- **Serial Peripheral Interface (SPI)**
  There are two general purpose 1-bit SPI masters. Software can preload the transaction, initiate it, and then either poll for completion or respond to the completion interrupt. Opcode, transaction type, data, and number of bytes are all software programmable. The hardware will serialize and sample incoming data as required by the protocol. The SPI port clock frequency is programmable and ranges from 7.8 kHz to 8 MHz.

- **UART**
  There are two UART cores with flow control present on the ATM2202. UART0 should be used for HCI type applications and UART1 primarily for debug messaging (without flow control).

- **PDM Digital microphone**
  PDM (Pulse Density Modulation) provides microphone support using two pins and supports three clock speeds (500 kHz, 1 MHz, and 2 MHz).

  The PDM-to-PCM conversion block takes as input a 1-bit PDM output from a digital microphone and outputs a 16-bit PCM signal at 16 kHz sample rate. The clock frequency to the PDM microphone can be selected to be 500 kHz, 1 MHz, or 2 MHz. The 1-bit PDM signal is filtered through a 3rd order sinc decimation filter to filter out ADC quantization noise. This is followed by a 1st order IIR filter (that can be bypassed) which attenuates any residual DC content. The corner frequency of the IIR filter is programmable. The gain control block has a programmable gain from -30 dB to 30 dB in steps of 0.5 dB. The output bit rate is 16 bit x 16 kHz = 256 kbps.
  The output from the PDM core is captured in a FIFO which supports a ping-pong type drain mechanism.

- **PWM**
  The PWM has eight independent pulse width modulation output channels. Each channel has frequency and duty cycle options. Additionally, all channels can be started at exactly the same time if synchronization is required. The frequency ranges from 250 kHz to 8 MHz and the duty cycle is tunable in 1/64th steps.

- **Quadrature Decoder for mouse inputs (QDEC)**
  The QDEC is a 3-axis (x,y,z) quadrature decoder. Each axis is independent and requires 2 input pins. QDEC continuously updates the internal integrators and their values can be read by software.

- **Keyboard Matrix Controller (KSM)**
  The KSM is a keyboard scanner which supports up to 3 rows by 7 columns or 7 rows by 3 columns. Key pressed and key released events can optionally require that the key be pressed or be released across multiple consecutive scans. Up to 12 simultaneous key events can be tracked.
  A portion of the KSM can continue to scan during low power states. The key pressed or key released event can also optionally wake the ATM2202 from a low power state. Key events are not lost when the ATM2202 is in a low power state. Key events are packetized and written into a FIFO via the hardware for later reading by the software.

- **Analog Comparator**
  A 16-level analog comparator provides an ultra-low power approach to sense an analog input signal from sensors.

- **Application ADC**
  10-bit Application ADC with 1 differential input or 3 single-ended inputs. The ADC input can be one of the input pins, internal signals such as temperature or voltage (supply, battery).   The selected input signal is digitized by 10-bit ADC at 2 Msps.

2 Electrical Specification

All parameters are based on 3 V supply at 25 °C unless otherwise specified.

Table 2-1   **Maximum Electrical Ratings**

Maximum Ratings					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
VBAT	Battery supply[2]	-0.2		3.6	V
VDDIO	I/O supply	-0.2		3.6	V
VIO	I/O pin (VDDIO > 3.4 V) I/O pin (VDDIO <= 3.4 V)	-0.2 -0.2		3.6 VDDIO+0.2	V V
VRF	RF I/O pin			10	dBm
ESD$_{HBM}$	ESD HBM (Class 2)			2000[3]	V
ESD$_{CDM}$	ESD CDM			500	V
T$_{STORE}$	Storage Temperature	-40		125	°C

Table 2-2   **Recommended Operating Conditions**

Recommended Operating Conditions					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
VDDIO	I/O supply	1.7	1.8	3.3	V
VBAT	Battery supply	1.1[4]		3.3	V
VPP25	OTP Programming Voltage[5]	2.3	2.5	2.7	V
VIO	I/O pin	-0.2		VDDIO+0.2	V
	Crystal (Tolerance + Stability) - 16.000 MHz	-50		50	ppm
	Crystal (Tolerance + Stability) - 32.768 kHz	-500		500	ppm

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[2] VBAT minimum slew rate is 0.3 V/ms

[3] Pins TMC and PWD are 1250 V

[4] VBAT minimum supply after boot is 1.0 V

[5] VPP25 is physically connected to VDDIO. Set VDDIO to within VPP25 range when programming the OTP.

	Internal RC (RCOSC) Frequency - 32.768 kHz[6]	30.5		35	kHz
TA	Operating (Ambient) Temperature	-40	25	85	°C

Table 2-3   Radio Transceiver Characteristics

Radio Transceiver Characteristics					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Frequency		2.402		2.480	GHz
Rx sensitivity	37-byte packets, clean Tx				
	125 kbps		-101		dBm
	500 kbps		-98.5		dBm
	1 Mbps		-95		dBm
	2 Mbps		-93		dBm
	255-byte packets, dirty Tx				
	125 kbps		-100		dBm
	500 kbps		-96.5		dBm
	1 Mbps		-94		dBm
	2 Mbps		-91		dBm
Tx output power	4, 2, 0, -2, -4, -6, -10, -20	-20		4	dBm
Tx power accuracy			+/- 4		dB
Tx spectral mask @ 1M sym/s	2 MHz offset	-20			dBm
	> 3 MHz offset	-30			dBm
Rx Carrier-to-Interferer (LE 1M PHY)	Co-channel interference	21			dB
	Adjacent 1 MHz interference	15			dB
	Adjacent 2 MHz interference	-17			dB
	Adjacent 3 MHz interference	-27			dB
RSSI resolution			1		dB
RSSI accuracy	-90 to -20 dBm		+/- 2		dB

Table 2-4   Wakeup Receiver Characteristics

Wakeup Receiver Characteristics					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**

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[6] RCPSC at room temperature.

Sensitivity[7]	915 MHz and 2440 MHz, 14-byte packets at 1 ms intervals for 40 ms		-44		dBm

Table 2-5   PMU Characteristics

PMU Characteristics					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
AVDD1P Output Voltage			1.0		V
DVDD1P Output Voltage			1.0		V
VDDIOP Output Voltage			1.8		V
VAUX Output Voltage			3.2		V

Table 2-6   GPIO Characteristics

GPIO Characteristics					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Input VIH		VDDIO-0.5		VDDIO	V
Input VIL		-0.2		0.2	V
Output VOH	2 mA Load		VDDIO-0.2		V
Output VOL	2 mA Load		0.2		V
Drive Strength - high drive (P20-P24)	VDDIO = 3.3 V VDDIO = 1.7 V		16 10		mA mA
Drive Strength - standard drive (all except P20-P24)	VDDIO = 3.3 V VDDIO = 1.7 V		8 5		mA mA
Pull-up Resistance	VDDIO = 3.3 V VDDIO = 1.7 V		45 100		kΩ kΩ

Table 2-7   Application ADC Characteristics

Application ADC Characteristics

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[7] >= 90% wakeup success rate

Parameter	Conditions	Min	Typ	Max	Unit
Resolution			10		bits
Sampling Rate	Without averaging		2		MHz
Temperature measurement accuracy			+/- 5		°C
Voltage measurement gain error			+/- 1		%
Voltage measurement offset error			+/- 2		LSB

Table 2-8   Embedded Flash Characteristics

Embedded Flash Characteristics					
Parameter	Conditions	Min	Typ	Max	Unit
Endurance	Program/Erase	100,000			Cycles
Data Retention			20		Year
Page Program Time			1		ms
Sector Erase Time			100		ms

Table 2-9   Power Consumption

Power Consumption VBAT current at 3 V with internally generated I/O supply					
Parameter	Conditions	Min	Typ	Max	Unit
Active RX	Sensitivity at -95 dBm		1		mA
Active TX @ 4 dBm	Output power at 4 dBm		4		mA
Active TX @ 0 dBm	Output power at 0 dBm		2.5		mA
Active TX @ -10 dBm	Output power at -10 dBm		1.4		mA
CPU Active	Executing CoreMark from RAM at 16 MHz		0.4		mA
CPU Idle + Bluetooth LE Deep Sleep			0.2		mA
Powerdown	PWD pin asserted		75		nA
Retention (32 KB RAM)			2		μA

Hibernation			0.8		µA
Hibernation with Wakeup Receiver			0.95		µA
SoC Off			300		nA

3   Signal Description

3.1   ATM2202 Pinout
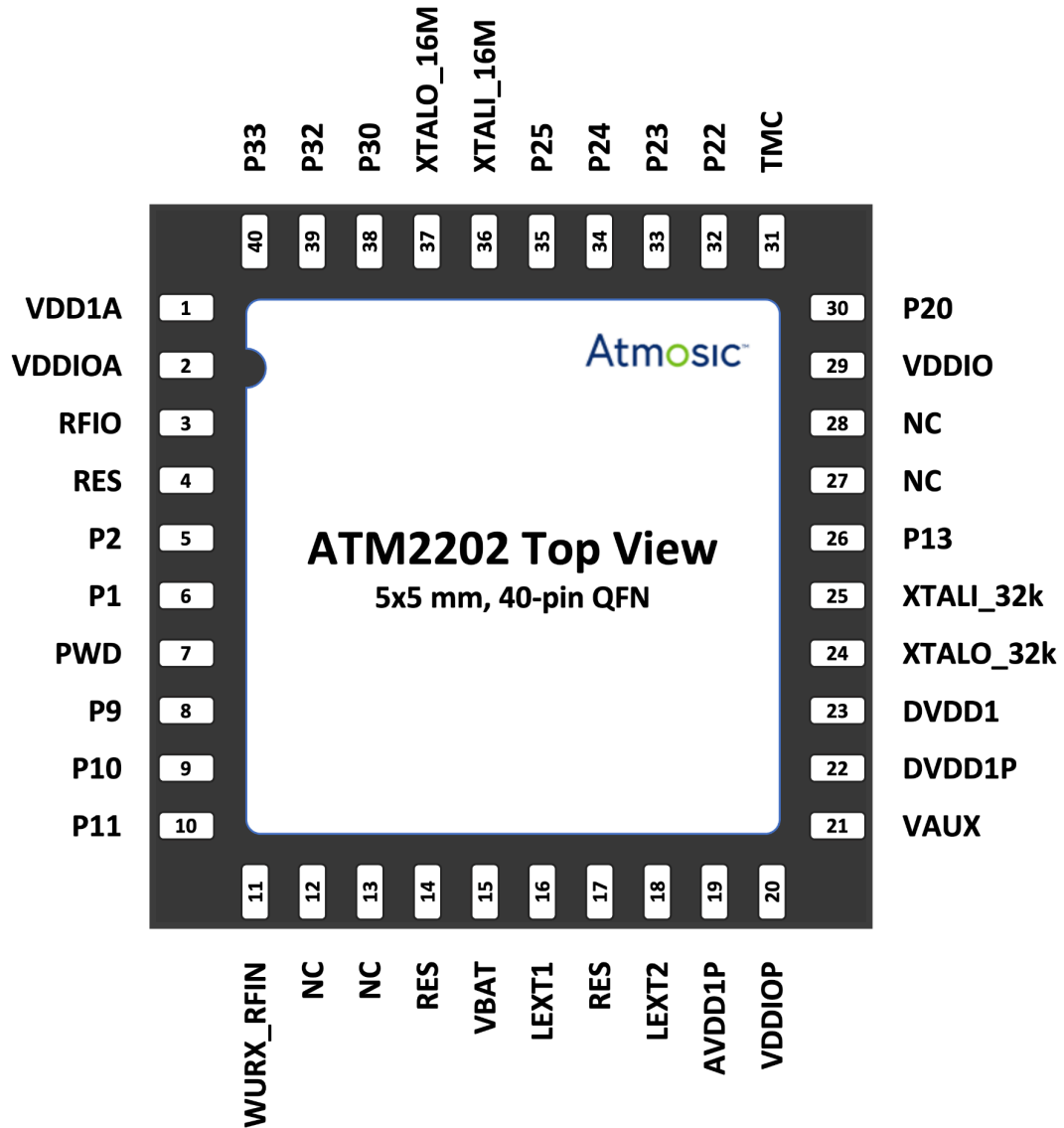
The ATM2202 is packaged in a 40-pin Quad Flat Package No Leads (QFN). The pin assignment is shown in . All pins are on the bottom side of the package.

Figure 3.1-1   **40-Pin QFN Pinout for ATM2202, Package Type 1 (Top View)**
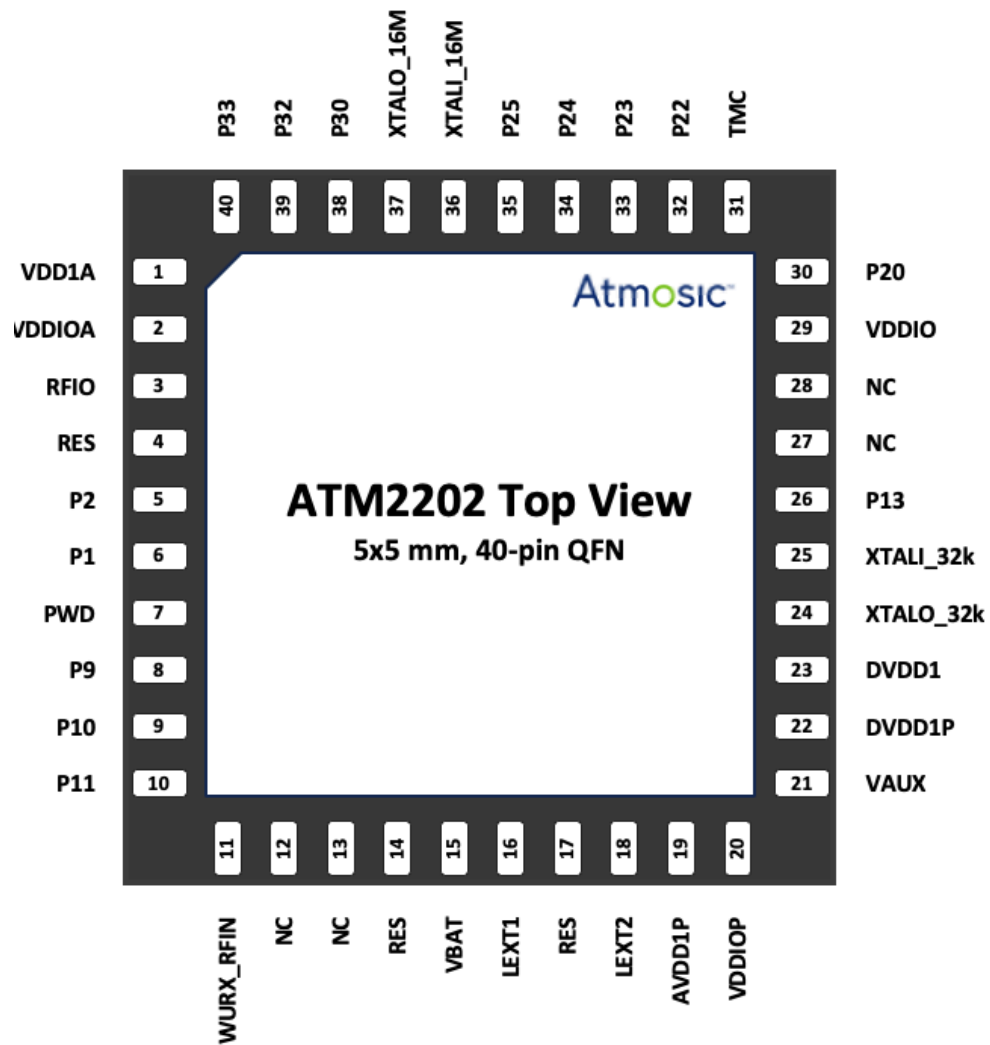
Figure 3.1-2   **40-Pin QFN Pinout for ATM2202, Package Type 2 (Top View)**

Pin Type Definitions	
Pin Type	**Definition**
I/O	Signal Input Output
RF	Radio Frequency

PWR	Power supply
A	Analog
R	Reserved
NC	No connection, must be open
GND	Ground

Table 3.1-1   ATM2202 Pin Description

ATM2202 Pin Description

Pin Number	Name	Type	Description
1	VDD1A	PWR	Analog and RF core power supply
2	VDDIOA	PWR	Analog and RF I/O power supply
3	RFIO	RF	2.4 GHz Single-ended RF I/O for Bluetooth radio
4	RES	R	Reserved, must tie to ground
5	P2	I/O	Serial wire debug data
6	P1	I/O	Serial wire debug clock
7	PWD	I/O	Power Down Input (Active High)
8	P9	I/O	Programmable Digital or Analog I/O (standard drive)
9	P10	I/O	Programmable Digital or Analog I/O (standard drive)
10	P11	I/O	Programmable Digital or Analog I/O (standard drive)
11	WURX_RFIN	RF	Wakeup receiver RF input
12	NC	NC	No connection, must be open
13	NC	NC	No connection, must be open
14	RES	R	Reserved, must tie to ground
15	VBAT	PWR	Battery supply
16	LEXT1	A	Switcher Inductor
17	RES	R	Reserved, must tie to ground
18	LEXT2	A	Switcher Inductor
19	AVDD1P	PWR	1 V Analog and RF core power supply generated by switcher
20	VDDIOP	PWR	1.8 V I/O power supply generated by switcher, connect to VAUX if unused
21	VAUX	PWR	Reserved for switching regulator internal use
22	DVDD1P	PWR	1 V Digital core power supply generated by switcher
23	DVDD1	PWR	1 V Digital core power supply
24	XTALO_32k	A	32.768 kHz crystal oscillator output
25	XTALI_32k	A	32.768 kHz crystal oscillator input
26	P13	I/O	Programmable Digital I/O (standard drive)
27	NC	NC	No Connection, must be open
28	NC	NC	No connection, must be open
29	VDDIO	PWR	Digital I/O Power Supply
30	P20	I/O	Programmable Digital I/O (high drive)
31	TMC	I/O	VDD_FLASH PWR Flash Power Supply must tie to VDDIO

32	P22	I/O	Programmable Digital I/O (high drive)
33	P23	I/O	Programmable Digital I/O (high drive)
34	P24	I/O	Programmable Digital I/O (high drive)
35	P25	I/O	Programmable Digital I/O (standard drive)
36	XTALI_16M	A	16 MHz crystal oscillator input
37	XTALO_16M	A	16 MHz crystal oscillator output
38	P30	I/O	Programmable Digital I/O (standard drive)
39	P32	I/O	Programmable Digital I/O (standard drive)
40	P33	I/O	Programmable Digital I/O (standard drive)
EPAD	VSS	GND	Ground supply for all circuits. The 40-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS.

4 Mechanical Drawing

Figure 4.1-1   40-Pin QFN ATM2202 Mechanical Drawing, Package Type 1
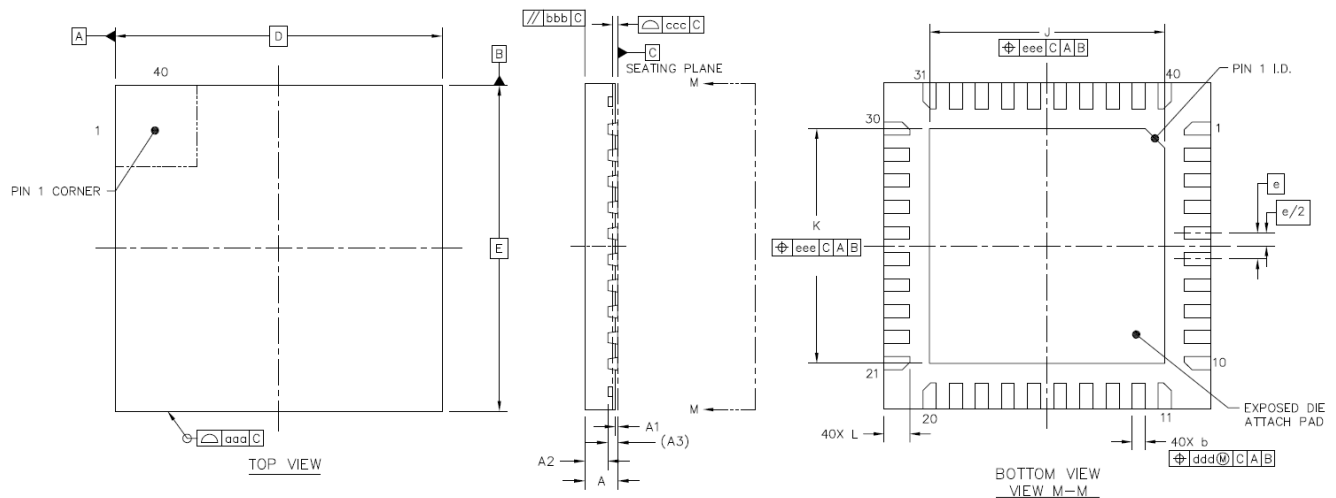
Table 4.1-1   40-Pin QFN ATM2202 Dimensions, Package Type 1

		Symbol	Min	Nom	Max
Total Thickness		A	0.80	0.85	0.90
Stand Off		A1	0	0.035	0.050
Mold Thickness		A2	---	0.65	0.67
L/F Thickness		A3		0.203 REF	
Lead Width		b	0.15	0.20	0.25
Body Size	X	D		5 BSC	
	Y	E		5 BSC	
Lead Pitch		e		0.4 BSC	
EP Size	X	J/D2	3.5	3.6	3.7
	Y	K/E2	3.5	3.6	3.7
Lead Length		L	0.35	0.40	0.45
Package Edge Tolerance		aaa		0.1	
Mold Flatness		bbb		0.1	
Coplanarity		ccc		0.08	
Lead Offset		ddd		0.1	
Exposed Pad Offset		eee		0.1	

Notes:

- All dimensions are in millimeters.
- Coplanarity applies to leads, corner leads, and die attached pad.

Figure 4.1-2   40-Pin QFN ATM2202 Mechanical Drawing, Package Type 2

TOP VIEW   SIDE VIEW   BOTTOM VIEW
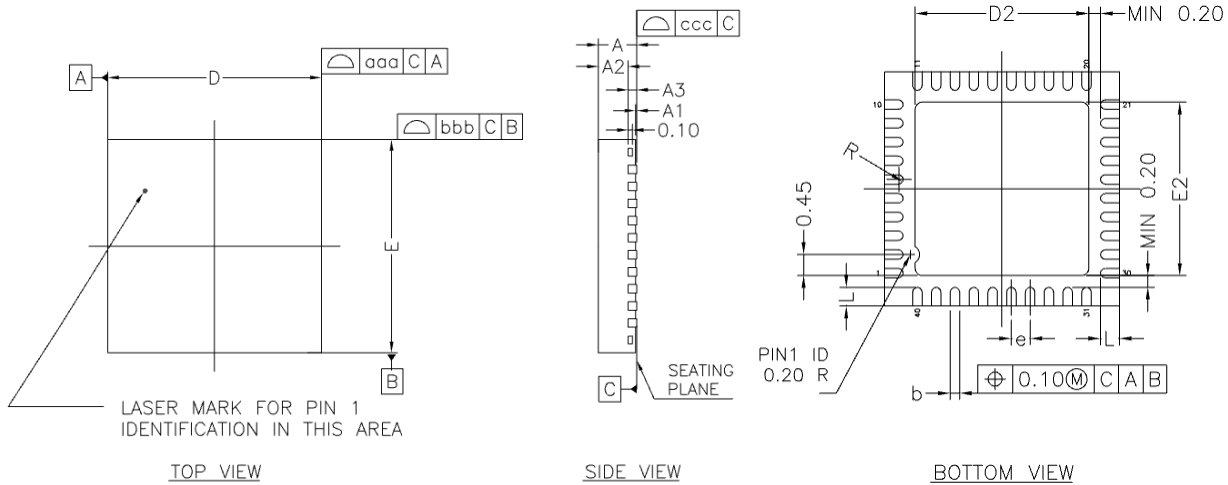
Table 4.1-2   40-Pin QFN ATM2202 Dimensions, Package Type 2

		Symbol	Min	Nom	Max
Total Thickness		A	0.8	---	0.9
Stand Off		A1	0	---	0.05
Mold Thickness		A2	---	0.65	0.70
L/F Thickness		A3	0.20 REF		
Lead Width		b	0.15	0.20	0.25
Body Size	X	D	5 BSC		
	Y	E	5 BSC		
Lead Pitch		e	0.4 BSC		
EP Size	X	D2	3.6	3.7	3.8
	Y	E2	3.6	3.7	3.8
Lead Length		L	0.35	0.40	0.45
Package Edge Tolerance - X		aaa	0.1		
Package Edge Tolerance - Y		bbb	0.1		
Coplanarity		ccc	0.05		

Notes:

● All dimensions are in millimeters.
● Coplanarity applies to leads, corner leads, and die attached pad.

5   Part Ordering

Table 5-1   Part Ordering Numbers

Part Number	Product Line	Description
ATM2202SR	Wireless MCU	5x5 40-Pin QFN ATM2202 Bluetooth 5.0 SoC with 1 MByte embedded flash, Tape and Reel, 7" Small Reel

Revision History

Date	Version	Description
September xx, 2024	1.14	Add Type 2 Package drawings
January 16, 2024	1.13	Corrected typos.
January 9, 2023	1.12	Updated Features section, Table 2-2 Recommended Operating Conditions.
September 3, 2022	1.11	Updated Part Ordering Numbers.
July 14, 2022	1.10	Updated Part Ordering Numbers.
April 20, 2022	1.00	Updated Table 2-7 Application ADC Characteristics, changed format of 40-Pin QFN Pinout for ATM2202 (Top View) pinout diagram, corrected typos.
April 1, 2022	0.57	Changed format, and corrected typos.
December 3, 2021	0.56	Updated System block diagram, 128 KB Flash not supported, GPIO Characteristics, ATM2202 Pin Description sections. Changed format.
August 16, 2021	0.55	Updated pin description of ATM2202 pin P30, P32, P33. Corrected typos.
April 17, 2021	0.54	Updated Electrical Specification, Part Ordering sections.
December 2, 2020	0.53	Corrected typos.
August 4, 2020	0.52	Updated CPU & Memory under SRAM, Added Table 2-4, removed Table 3-3, Updated Table 2-1, Table 2-7, and various sections.
March 22, 2020	0.51	Corrected typos, updated Figure 1-1, Figure 3.1-1.
March 13, 2020	0.50	Initial version created.

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