Hardware Design Guide for ATMx2xx

Revision History

Date	Version	Description
November 7, 2019	0.50	Initial version created.
February 14, 2020	0.51	Updated PMU Configuration and Component Selection sections.
July 2, 2020	0.52	Updated Power Management Unit (PMU) configuration, Connection tips, Layout guidelines sections, added RF Harvester storage capacitor, RF Harvester Section, Matching Guidelines sections.
August 10, 2020	0.53	Updated Power Management Unit (PMU) configuration, Connection tips, Component selection sections.
November 20, 2020	0.54	Updated Connection tips, Flash, RF front-end module support sections
December 2, 2020	0.55	Corrected typos.
March 30, 2021	0.56	Updated Connection tips, Flash, 16 MHz crystal, 32.768 kHz crystal, RF Harvester storage capacitor sections, and bullet regarding RC filter placement,
April 14, 2021	0.57	Updated format, no content change.
July 15, 2021	0.58	Updated Flash, Switcher Inductor, Layout Guidelines, and Matching Guidelines sections.
April 6, 2022	0.59	Updated Connection tips, Flash sections, added Figure 3c - RF Harvesting Matching Circuit for ATM3231.
January 24, 2023	0.60	Updated Connection tips section.
November 22, 2024	0.61	Updated Connection tips section.

Table of Contents

List of Figures

List of Tables

1 Overview

The ATM32xx/ATM22xx are part of a family of extremely low-power Bluetooth® 5 system-on-a-chip (SoC) solutions. This Bluetooth Low Energy SoC integrates a Bluetooth 5.0 compliant radio with ARM® Cortex® M0 application processor, 128 KB Random Access Memory (RAM), 256 KB Read Only Memory (ROM), 4 KB One-Time-Programmable (OTP) memory, and state-of-the-art power management.

This document describes how to implement hardware designs with these parts:

- ATM3201
- ATM2201
- ATM3202
- ATM2202
- ATM3221
- ATM2221
- ATM3231
- ATM2231
- ATM2251

The following topics are covered:

- Power Management Unit (PMU) configuration
- Digital IO connections
- Component selection
- Layout guidelines
- Matching guidelines

2 Power Management Unit (PMU) Configuration

Please refer to the "PMU configurations" section of the ATMx2xx Reference Manual for configuration and schematic details. When using the Software Development Kit (SDK), the PMU_CFG makefile argument will program the PMU configuration fields in software or the hardware One Time Programmable (OTP) memory depending on the makefile target.

Choosing the appropriate IO supply configuration depends on the following factors:

1. VBAT source
   If the ATM32xx is operating without a battery, the IO supply must be internally generated.

2. VBAT voltage level
   VBAT must be either between 1.1 V and 1.8 V or between 1.8 V and 3.3 V. If VBAT is between 1.1 V and 1.8 V, the IO supply must be internally generated. If VBAT is between 1.8 V and 3.3 V, the IO supply can either be internally generated, tied to VBAT, or connected to an external supply.

3. IO voltage level
   If the ATM2/ATM3 is interfacing to peripherals (e.g. flash, sensors, etc), they must share an IO supply. If any peripheral does not support a 1.8 V IO supply, the IO supply must be tied to VBAT or connected to an external supply.

4. Powering peripherals
   The ATM2/ATM3 can power peripherals from its internally generated IO supply up to an average of 10 mA and a peak of 20 mA. If the combined current consumption of all peripherals exceeds an average of 10 mA or a peak of 20 mA, the IO supply must be tied to VBAT or connected to an external supply. Note that if the application uses SoC Off, the IO supply will not be maintained during that low power mode.

5. External inputs
   If the application uses PWD, P10 for GPIO wakeup from SoC Off, or P11/P12 for analog comparator wakeup from Soc Off, the IO supply must be tied to VBAT or connected to an external supply.

3 IO Connections

All of the ATM2/ATM3 digital IO have programmable functionality, and using the Atmosic Pinmux Tool in the SDK is recommended for selecting digital IO functionality. The following sections cover some additional considerations:

3.1 Production test support

The production test setup needs access to the following IO:

- VDDIO/VDDIOA to supply 2.5 V to the DUT for OTP programming
- VBAT if it is not connected to VDDIO/VDDIOA
- GND
- PWD for resetting the DUT
- P32 for configuring the DUT to CPU idle state
- P1 and P2 for SWD to program the DUT
- UART0 for RF testing via DTM (2-wire) or HCI (4-wire) interface

If the design cannot allow the production test setup to supply 2.5 V to VDDIO/VDDIOA for OTP programming, the following ATM2/ATM3 functionality will be unavailable:

- Operation without external 32 kHz crystal
- OTP write protection
- Serial Wire Debug (SWD) disable
- RF Front End Module (FEM) support

3.2 Connection Tips

- For ATMx2x1 designs, Test Mode Control (TMC) can be tied high if P0, P1, and P2 are dedicated to debug functionality; otherwise, TMC should be pulled low.
- Power Down (PWD) requires a weak pull-down resistor and should not be tied to the ground. This allows SDK and production test tools to drive this pin as needed to reset the ATM2/ATM3. Pulses of voltage greater than VDDIO - 0.5 V and greater than 100 us in duration are recommended when this pin is used for resetting the chip.
    - For applications where VBAT can be disconnected or experience large voltage fluctuations for short periods, a PWD circuit (such as what is shown in Figure 1) is

recommended to ensure the ATM2/ATM3 resets properly.

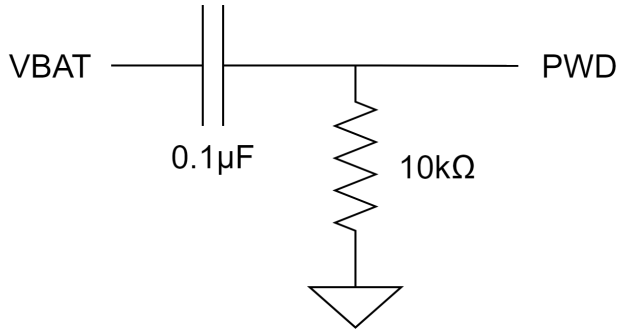

Figure 1 - Circuit to generate PWD Pulse

Note that due to board parasitics, component variations, and battery characteristics (voltage, drive strength), these values may need to be tuned to achieve the required pulse voltage and duration. Also, this circuit may generate a negative pulse when the VBAT voltage drops, but the PWD pin can tolerate it as long as the pin voltage does not drop below -1V.

- If P0 is needed for non-debug functionality, it needs to be pulled or driven low whenever TMC is asserted. Otherwise, P0 can be tied low.
- P32 requires a weak pull-down resistor and should not be tied to the ground. This allows SDK and production test tools to drive this pin as needed to put the CPU into an idle state. After the CPU boots, P32 can be reconfigured and used as a normal GPIO.
- For ATMx2x1 applications that use external IO supply, flash, and SoC Off or Powerdown, the flash CS pin may need to be pulled up to minimize flash power consumption during those low power modes. Please contact Atmosic Support to discuss applications that use external IO supply and SoC Off or Powerdown.
- All ATM2/ATM3 digital IO except P4-P7, P14-P20, and P22-P24 have a typical drive strength of 8 mA at 3.3 V IO and 5 mA at 1.7 V IO. P4-P7, P14-P20, and P22-P24 have a typical drive strength of 16 mA at 3.3 V IO and 10 mA at 1.7 V IO. As a result, some LEDs and sensors can be powered directly by ATM2/ATM3 digital IO.
- Any ATM2/ATM3 digital IO can be programmed to have an internal pull-up regardless of its selected functionality. The typical resistance is 45 kΩ at 3.3 V IO and 100 kΩ at 1.7 V IO. Note that if the application uses SoC Off, the internal pull-up will not be maintained during that low power mode.

- The default hardware state for most ATM2/ATM3 digital IO is high-Z. The exceptions are P14-P19 which defaults to QSPI, P32 which defaults to GPIO input, and P0-P2 which defaults to SWD if TMC is high.

- For ATM3 to demonstrate how much energy can be harvested under certain circumstances, a harvesting meter application can be implemented to display harvested energy in real-time. A GPIO pin should be connected to VSTORE for this functionality. Please refer to the ATM32x1 Harvesting Meter Application Note for more details.

- When the Application ADC is measuring an external analog signal, the internal impedance will vary depending on the voltage level. If an external resistor divider is being used, please contact Atmosic Support to discuss the impact of the internal impedance. If a transistor is being used to enable the Application ADC circuit, please ensure that the ATM2/ATM3 IO is pulled low when the transistor is off.

4 Component Selection

4.1 Flash

The flash used on the ATMx2x1 Evaluation Board (EVB) is the MX25R4035FM1IH1 from Macronix. It was selected to minimize system power consumption and maximize system performance. The ATMx2x1 supports the following serial flash families:

- Macronix MX25R
- Micron N25Q (not for new designs)
- Winbond W25QxxEW and W25QxxJW-xQ
- Gigadevice GD25WQ (the ATMx2x1-x0x requires the extra_flash SDK example programmed into OTP). Refer to the ATMx2xx Chip Revisions Application Note for information on chip revisions.
- Fudan Micro FM25W (requires the extra_flash SDK example programmed into OTP)
- Giantec GT25Q (requires the extra_flash SDK example programmed into OTP)
- Puya P25QxxU (only supported on ATMx2x1-x1x and requires the extra_flash SDK example programmed into OTP).

4.2 16 MHz Crystal

The 16 MHz crystal used on the ATM2/ATM3 EVB is the ECS-160-8-36-JTN from ECS (+/-20 ppm tolerance, +/-20 ppm stability, 8 pF load capacitance, 80 Ω maximum ESR). This can be used as a reference when choosing alternate parts (e.g. Epson FA-20H 16.0000MF20X-AJ or Abracon ABM10W-16.0000MHZ-8-D1X-T3). The ATM2/ATM3 supports up to +/-50 ppm total combined stability and tolerance as required by the Bluetooth 5 specification. The ATM2/ATM3 can support load capacitance up to 12 pF with internal tuning capacitors, but < 9 pF is recommended for lower power consumption.

If an alternate part with a different load capacitance is used, the ATM2/ATM3 internal tuning capacitors may need to be adjusted. This can typically be done via lab characterization:

1. Follow the instructions in the RF Tool User Guide to install and run the Atmosic RF Tool.
2. Connect the DUT RF port to a spectrum analyzer.
3. Select the CAL. tab on the Atmosic RF Tool, and click the “16MXtal Cal.” button. For each iteration, check the frequency offset on the spectrum analyzer, enter the value (Hz) in the pop-up window, and click Exit. Upon completion, the characterized value between 0 and 31 will be displayed in the Atmosic RF Tool.
4. Repeat steps #3 through #6 on a handful of DUTs to confirm that the characterized value is similar across multiple devices.

5. Input the characterized value into the Atmosic Production Test Tool to be programmed during DUT manufacturing.

If a TCXO is used, its output swing must be between 0 and 1 V. The output should be connected to the XTALI_16M pin, the XTALO_16M pin should be left floating, and the extclk bit in the CMSDK_PSEQ->XTAL_BITS1 register should be set.

4.3 32.768 kHz Crystal

The 32.768 kHz crystal used on the ATM2/ATM3 EVB is the ECS-327-7-12R from ECS (+/-20 ppm tolerance, 7 pF load capacitance, 70 kΩ maximum ESR). This can be used as a reference when choosing alternate parts (e.g. Micro Crystal AG CM8V-T1A-32.768KHZ-7PF-100PPM-TA-QC). The ATM2/ATM3 supports up to +/-500 ppm total combined stability and tolerance as required by the Bluetooth 5 specification. The ATM2/ATM3 can support load capacitance up to 12 pF with internal tuning capacitors, but < 9 pF is recommended for lower power consumption. Please note that the ATM2/ATM3 requires high impedance between the XTALI_32k and XTALO_32k pins, so it is recommended to minimize the use of solder flux when mounting the crystal.

If the application does not require a crystal, the XTALI_32k pin should be grounded, and the XTALO_32k pin should be left floating.

4.4 Switcher Inductor

The 4.7 µH multilayer chip power inductor used by the switcher on the ATM2/ATM3 EVB is the LQM2MPN4R7MG0L from Murata. The DC Resistance (DCR) of this inductor is 140/175 mΩ (typical/max), and its rated current is 1.1 A. If choosing an alternate part (e.g.Taiyo Yuden CKP20164R7M-T), it is recommended to have a similar DCR as this inductor, and a rated current of 500 mA or higher.

4.5 RF Front-End Module Support

The ATM2/ATM3 can output transmit and receive control signals to interface to an RF front-end module with an external power amplifier (external low-noise amplifiers are not supported). Pins for the control signals (XPAON Tx and Rx) can be selected using the Atmosic Pinmux Tool in the SDK. Applications should use the atm_ble_set_xpa function in the SDK to enable the control signals.

The external power amplifier gain must be input into the Atmosic Production Test Tool to be programmed during DUT manufacturing. The ATM2/ATM3 uses the external_pa_gain field in the CUST_CFG OTP tag to adjust the requested transmit power by the amount specified in the field

in dB. For example, the ATM2/ATM3 EVB has been validated with a SKY66407-11 evaluation board with external_pa_gain = 13.

4.6 RF Harvester Storage Capacitor

The EVBs have a 220 µF, or 220+100 µF storage ceramic capacitor(s) on VSTORE. The 220 µF capacitors have an effective capacitance of, approximately, 90 µF at 3.0 V. Similarly, the 100 µF capacitor also has a derating of roughly 56 % at 3.0 V, thereby having a C of about 55-60 µF at 3.0 V. Refer to Murata's datasheet.

The capacitance value of a high dielectric constant type capacitor changes depending on the DC voltage applied. Please consider this when choosing the amount of storage capacitance needed for the application.

Note: The EVB schematics have two Schottky diodes - D1 and D2. The EVBs currently have 0 Ω and 560 Ω resistors populated in their place, respectively. The Schottky diode D1 on the HARV_OUT pin is used in anticipation of multi-mode harvesting support at some point in the future. For now, the part has been substituted with a 0 Ω resistor. The Schottky diode D2, however, should be substituted with a 560 Ω resistor and is required for rechargeable battery operation.

Besides ceramic capacitors, supercapacitors can also be used as high-capacity storage capacitors. The following supercapacitors have been characterized with ATM32xx. Due to their intrinsic property of high internal resistance, it is recommended to have a 220 µF ceramic capacitor connected in parallel with the supercapacitor to mitigate the voltage ripple. This filtering ceramic capacitor is necessary for systems with supercapacitors only and no battery.

- Korship SM3R3333 (33 mF)
- Korship SM3R3703 (70 mF)
- ELNA DSK-3R3H334T (0.33 F)
- ELNA DSK-3R3H204T614 (0.2 F)

Korship datasheet
ELNA datasheet

Please consult Atmosic for the support of other supercapacitors.

5 Layout Guidelines

This section describes layout guidelines to be followed on some key signals/routes to/from ATM2/ATM3.

5.1 RFIO (Bluetooth LE) Section

The ATM2/ATM3 EVBs have a matching circuit as shown in Figure 2:

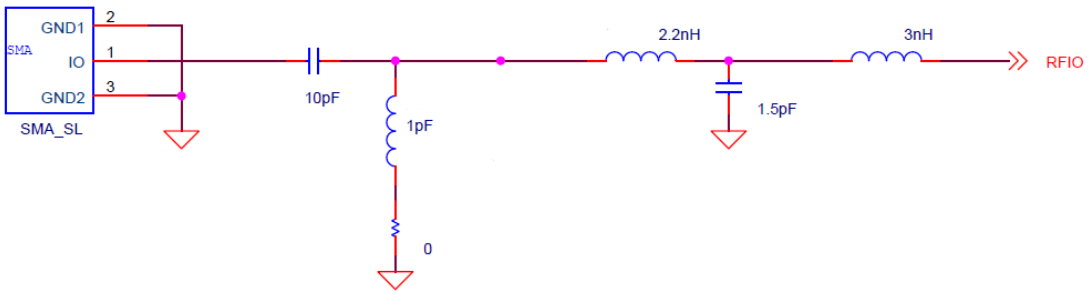

Figure 2 - RFIO (Bluetooth LE) Matching Circuit

The two series inductors (2.2 nH and 3 nH) and two shunt capacitors (1 pF and 1.5 pF) function as a lowpass filter (assuming a pure 50 Ω termination at all harmonic frequencies) to reject higher harmonic frequencies to meet FCC requirements. For the ATMx20x EVB, the 0 Ω resistor acts as a small inductor (0.2 nH) to resonate with the 1 pF capacitor to improve rejection of the 5th harmonic. This resistor is not needed for other designs. To ensure even more margin on the 5th harmonic, it is recommended that type MHQ inductors from TDK be used. If an antenna with good inherent harmonic rejection is used, this filtering network may be simplified. The series 10 pF capacitor functions as a DC block.

As for the placement on the PCB, the components shall be placed next to each other, minimizing connecting traces as much as possible.

The layout of the EVB PCB has this transmission line modeled as a CPW with a characteristic impedance of 50 Ω. The trace width/spacing can be adjusted according to the board stack-up.

5.2 Wakeup Radio Section

Figure 3 below shows a representative matching network for the Wakeup Radio on the ATM2/ATM3 EVBs. The corresponding component values and reference designators are tabulated in Table <n>.

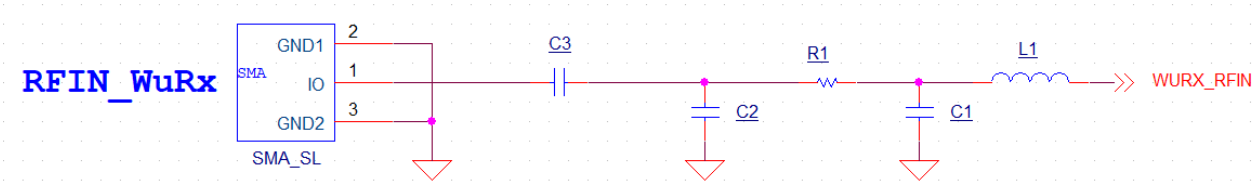

Figure 3 - Wakeup Radio Matching Circuit

EVB/Board	Part reference in Figure 2	Corresponding reference designator on the EVB	Value
ATMx20x (5x5) EVB	L1	L16	1.8 nH
	C1	C31	3.6 pF
	R1	R61	0 Ω
	C2	R65	NL
	C3	R60	0 Ω
ATMx221 (6x6) EVB	L1	R38	0 Ω
	C1	C30	NL
	R1	L5	0 Ω
	C2	C29	2.7 pF
	C3	C28	1.5 pF
ATMx231 (7x7) EVB	L1	R38	1.8 nH
	C1	C30	3.6 pF
	R1	L5	0 Ω
	C2	C29	NL
	C3	C28	0 Ω

As it can be seen, this is a two-element match. The 0-Ω series elements and the shunt element with no component loaded can be removed for area-sensitive designs.

As for the placement on the PCB, the components shall be placed next to each other.

The layout of the EVB PCB has this transmission line modeled as a CPW with a characteristic impedance of 50 Ω. The trace width/spacing can be adjusted according to the board stack-up.

5.3 RF Harvester Section

The ATM3 EVBs have a matching circuit as shown in Figure 4a, Figure 4b, and Figure 4c:

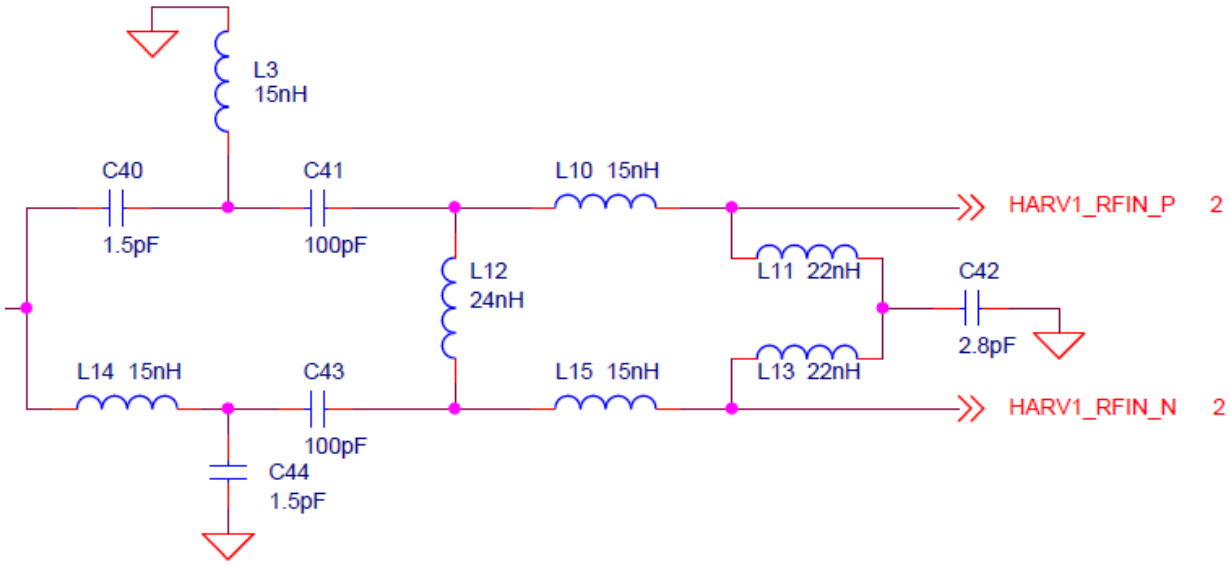

Figure 4a - RF Harvesting Matching Circuit for ATM320x

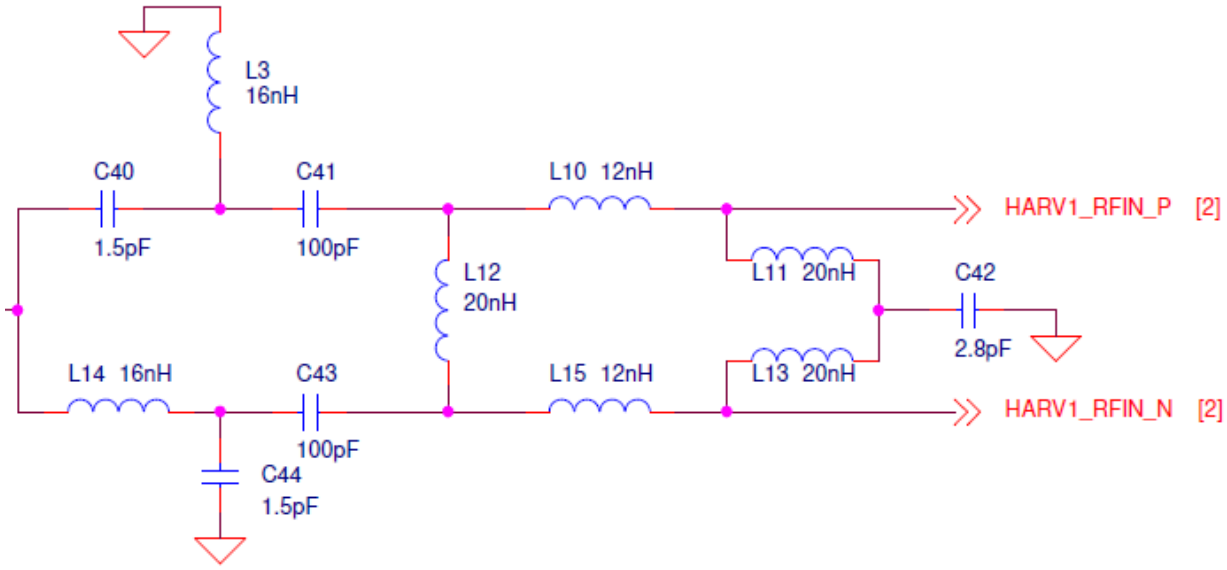

Figure 4b - RF Harvesting Matching Circuit for ATM3221

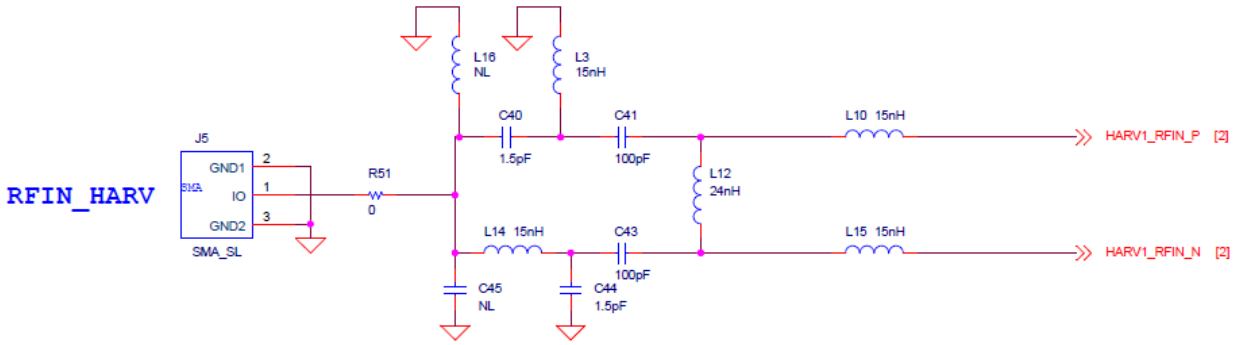

Figure 4c - RF Harvesting Matching Circuit for ATM3231

It is recommended to follow the below layout recommendations:

- The trace from the antenna to the harvester matching circuit shall have a characteristic impedance of 50 Ω.
- As for the placement on PCB, the components shall be placed next to each other with the chip-facing component (L10/L15 in the case of EVBs) placed as close as possible to the chip pins.
- On ATM320x-based PCBs with the 5x5mm QFN package, the routing from chip pins 12 and 13 is done in the following way:

    - Pins 12 and 13 are routed out with 5-mil thin traces until the SMD pads of the first component closest to the chip (L10/L15 in EVBs). These traces should be kept as short and as thin as possible to minimize the shunt capacitance presented to the chip pins 12 and 13 as well as the series inductance connecting the matching circuit. These traces should be equal in length.

- On ATM3221-based PCBs with the 6x6mm DRQFN package, the routing from the chip pins A12 & B9 is done in the following way:
    - Pins A12 and B9 are routed out with 3-mil thin traces (to escape the inner row of the package) until the SMD pads of the first component closest to the chip (L10/L15 in EVBs). These traces should be kept as short and as thin as possible to minimize the shunt capacitance presented to the chip pins 12 and 13 as well as the series inductance connecting the matching circuit. These traces should be equal in length.

- On ATM3221-based PCBs with the 7x7mm QFN package, the routing from chip pins 19 and 20 follows the same guidelines as those described above for the ATM320x-based PCBs.
- For 2-layer PCB designs, the ground underneath the matching components should be as solid and continuous as possible.

- Place the 10 µF capacitor on HARV_OUT close to the IC pin (14). Priority should be given to the matching components, but this capacitor should not be far from the chip pin.
- Please refer to the PCB layouts under the “HW Reference Designs” link for better understanding.

5.4 Board Stack-up

While the board stack-up can be chosen according to the needs of the application, the stack-up of the current version of ATM2/ATM3 EVBs is shown in Figure 5. The board thickness is 62 mils (or, 1.58 mm) in either case.

Figure 5 - Board Stack-Up

Also, shown in Figure 6 is another example of a 4-layer stack-up for thinner (32 mils/0.8 mm) PCBs.

PCB STACK UP 4-layer			
		Layer Name	Thickness 0.8 mm
	SM		0.6
TOP	L1	1/2 oz+plating	1.7
		PP:2116	4.98
GND	L2	1oz	1.2
		core: 15mil	15
GND	L3	1oz	1.2
		PP:2116	4.98
BOT	L4	1/2 oz+plating	1.7
	SM		0.6
		Total	31.96 mil

Figure 6 - Another 4 -Layer Stack-up for Thinner PCB

5.5 Switcher Inductor

For ATMx221-based 4-layer PCBs with the 6x6mm DRQFN package that have single-sided SMD components, such as the ATMx221 EVB, the 4.7 µH switcher inductor needs to be placed as close as possible to pins B12 & B13. However, priority is given to the decoupling capacitor connected to pin A18 (AVDD1P). The traces between the pins B12 & B13, and the inductor shall be routed on an inner/bottom layer through vias for a lower trace resistance. The vias near pins B12 & B13 shall be placed within the chip boundary. Vias with a drill size of 10 mils is recommended. A trace width of at least 10 mils is recommended and minimizes the loop area formed by the traces, inductor, and chip. Avoid any routing on all layers beneath the inductor. Figure 7 illustrates a recommended layout for the above-mentioned guideline.

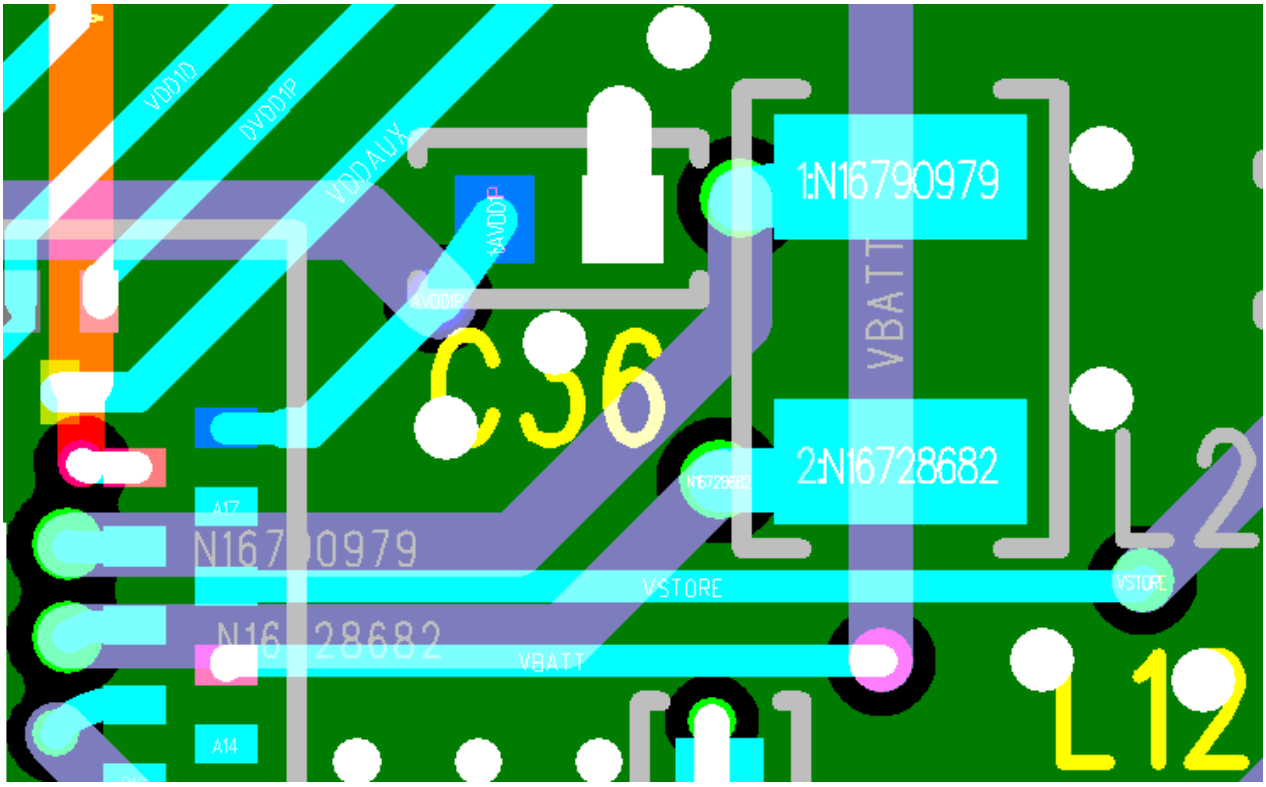

Figure 7 - Switcher Inductor Layout Recommendation for ATMx221 PCB with Single-sided SMD Components

For ATMx221-based PCBs that have double-side SMD components, the inductor shall be placed very close to the vias that are dropped from pins B12 & B13, as shown in Figure 8. Follow the above recommendations for trace width and via size.

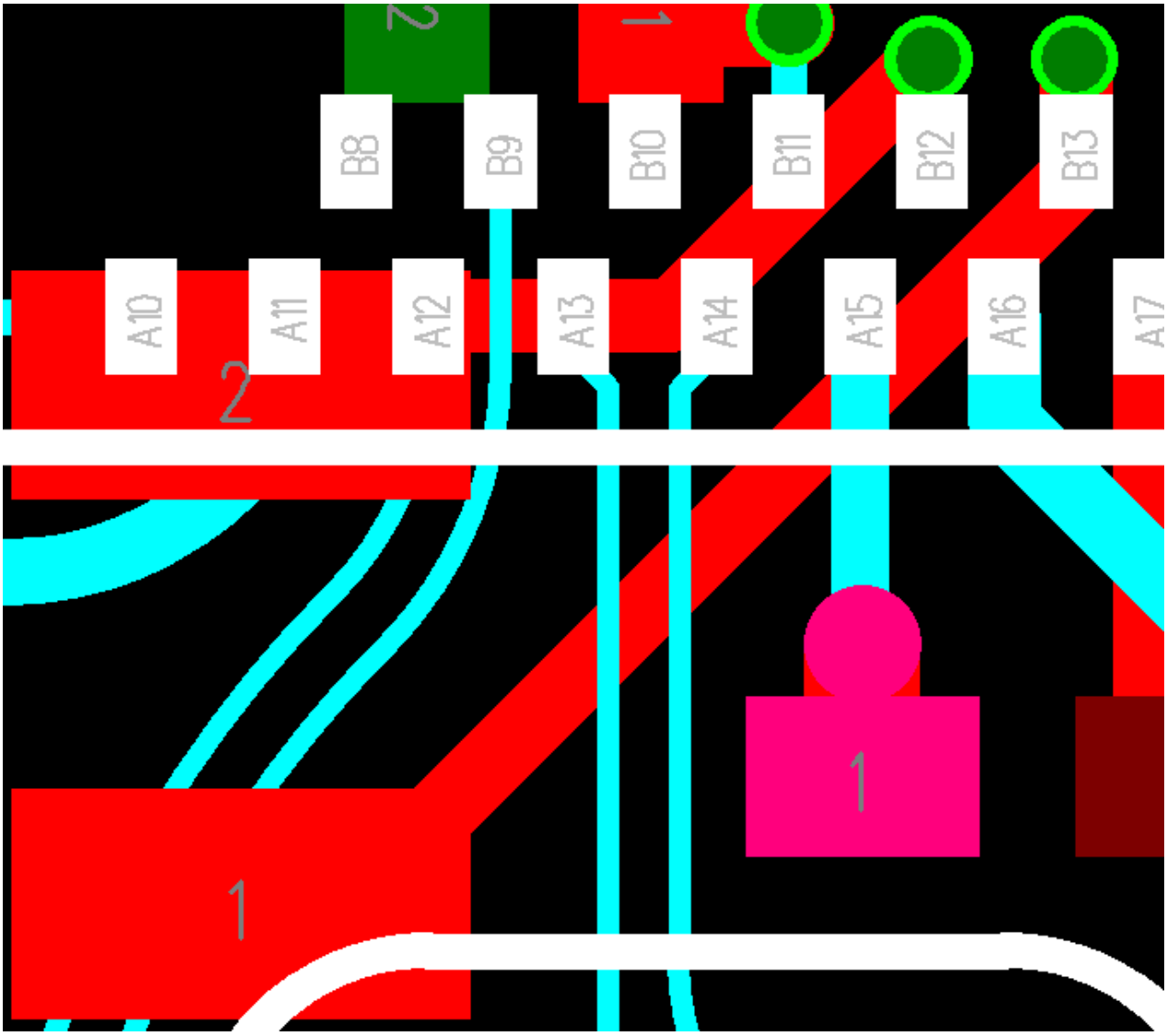

Figure 8 - Switching Inductor Layout Recommendation for ATMx221 PCB with Double-sided SMD Components

For ATMx20x-based 4-layer PCBs with the 5x5mm QFN package or ATMx231-based 4-layer PCBs with the 7x7mm QFN package that have single-sided SMD components, such as the EVB, the 4.7 µH switcher inductor needs to be placed as close as possible to pins 16 & 18 (for ATMx20x) or pins 23 & 25 (for ATMx231). However, priority is given to the bypass caps connected to pin AVDD1P (pin 19 for ATMx20x or pin 26 for ATMx231), and pin VBATT (pin 15 for ATMx20x or pin 22 for ATMx231). If the traces between pins 16 & 18 (for ATMx20x) or pins 23 & 25 (for ATMx231) and the inductor are routed on an inner/bottom layer through vias, for lower total resistance, via drill size of at least 10 mils and trace width of at least 10 mils are recommended and the loop area formed by the traces, inductor, and chip should be minimized. Avoid any routing on all layers beneath the inductor. If these traces are routed on the top layer

(on the ATMx231-based EVB), they should be kept as short and as wide as permitted. Figure 9 illustrates a recommended layout for the above-mentioned guideline.

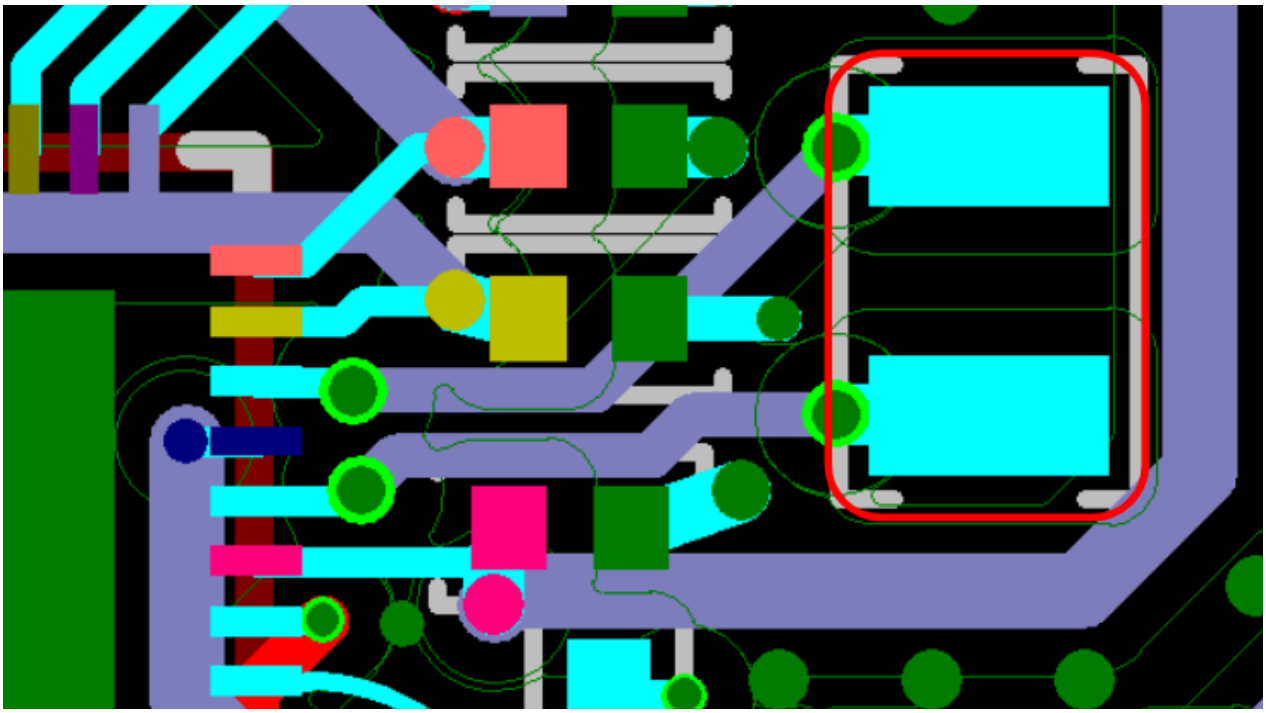

Figure 9 - Switcher Inductor Layout Recommendation for 4-layer ATMx20x PCB with Single-sided SMD Components

For ATMx20x-based PCBs that have double-sided SMD components, the inductor shall be placed very close to the vias that are dropped from pins 16 & 18. Follow the above recommendations for trace width, and via size.

For ATMx20x-based 2-layer PCBs with the 5x5mm QFN that have single-sided SMD components, the inductor shall be routed on the top layer with solid grounding below the inductor and also between the inductor & LEXT1|2 pins. The AVDD1P and VBATT bypass capacitors shall then be placed adjacent to the inductor, with the ground between the inductor and capacitor terminals. An example illustration is shown below in Figure 10.

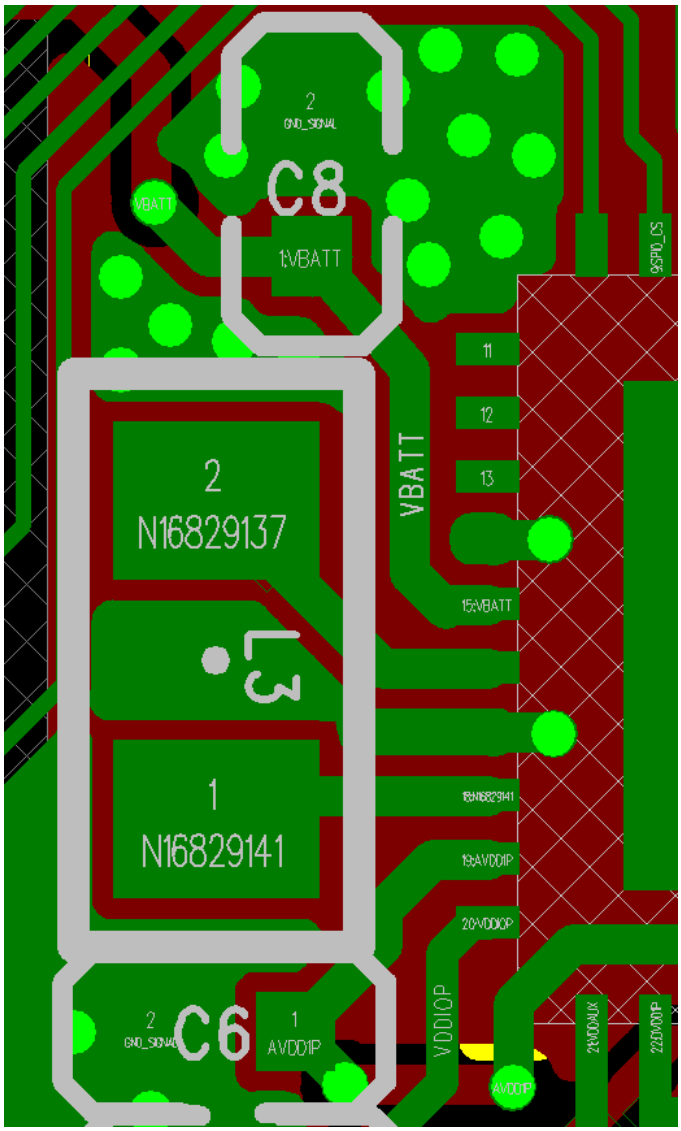

Figure 10 -Switcher Inductor Layout Recommendation for 2-layer ATMx20x PCB with Single-sided SMD Components

5.6 Analog Supply (AVDD1P & VDD1A)

The placement of bypass capacitors on the analog rail, and its routing from the AVDD1P pin to the VDD1A pin is critical to the performance of the PMU and radio blocks.

- Place the 10 µF bypass cap on AVDD1P as close as possible to the pin (pin 19 on ATMx20x-based PCBs with 5x5 QFN, or pin A18 on ATMx221-based PCBs with the 6x6mm DRQFN package, or pin 26 for ATMx231-based PCBs with the 7x7mm QFN package. This capacitor must be placed on the same layer as the ATM2/ATM3 chip.

- While routing AVDD1P to VDD1A via the RC filter, place the via closer to the AVDD1P bypass capacitor than to the pin/pad itself. In doing so, the AVDD1P pin “sees” less inductance (thus lower impedance) to the bypass capacitor than to the remaining trace.

- In ATMx20x-based PCBs with the 5x5 mm QFN, the AVDD1P trace can be routed as done in the EVBs, as shown in Figure 11 (see lavender trace). Notice also that this trace is routed around the crystal to avoid cutting through the crystal traces and picking up crystal noise.

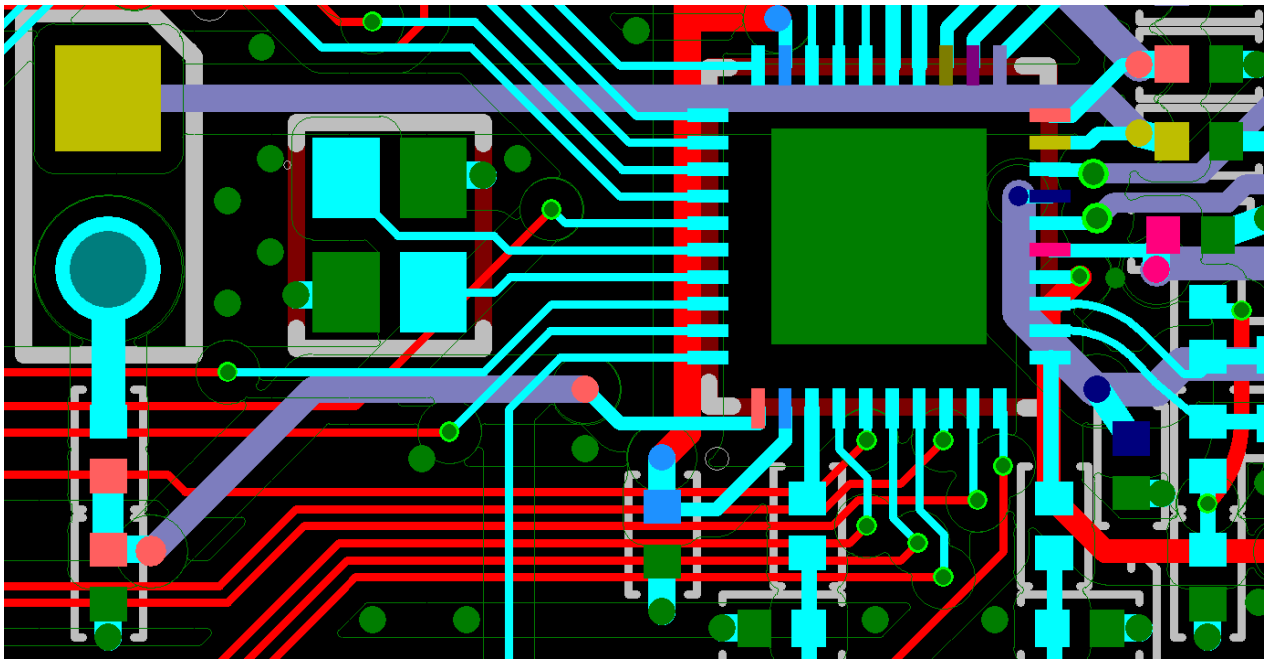

Figure 11 - AVDD1P trace Layout Recommendation for 4-layer ATMx20x PCB with Single-sided SMD Components

- Alternatively, in constrained designs such as a 2-layer PCB, AVDD1P trace can also be routed, for the most part, in the top layer sandwiched between the GND paddle and SMD pads, as shown in Figure 12 (see highlighted section in yellow). It is recommended to have a 7-8 mils clearance on either side of the trace.
-

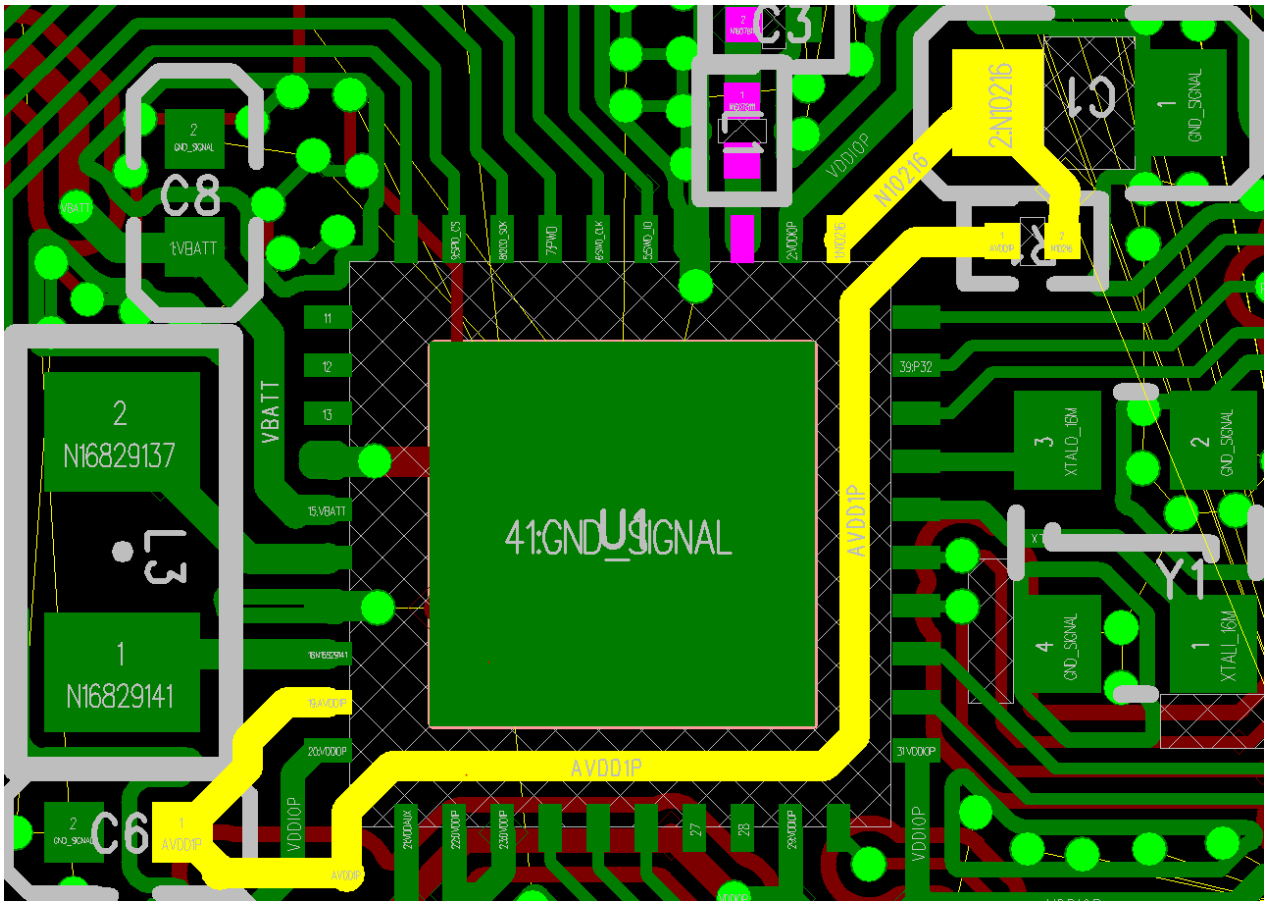

Figure 12 - AVDD1P trace Layout Recommendation for 2-layer ATMx20x PCB with Single-sided SMD Components

- Place the RC filter (1 Ω+10 µF) close to the VDD1A pin (pin 1 on ATMx20x-based PCBs with the 5x5 mm QFN package and ATMx231-based PCBs with the 7x7mm QFN package, or pin B1 on ATMx221-based PCBs with the 6x6 mm package DRQFN) to filter out effectively any noise that may get on the AVDD1P supply trace. The VDD1A supply should be within +/- 5% for performance and +/- 20% for functionality. Placing the capacitor < 3 mm from the VDD1A pin should be enough to keep the parasitic inductance < 3 nH.

5.7 ATM2251 (Chip Scale Package)

The ATM2251 EVB consists of a smaller (15x15 mm package) Module Board soldered on a larger Carrier Board. This Module Board can serve as a reference guide for placement and routing for ATM2251 PCBs.

- The ATM2251 Module Board is a 6-layer PCB with via-in-pads (T/H) under several bumps. For PCB layout and stack up, please refer to the ATM2251-Module_revA1_PCB directory in the Customer portal.

- Place critical components such as the switcher inductor, decoupling capacitors (on AVDD1P, DVDD1, VDDIOP, VBATT, VDDAUX), and RC filter (on VDD1A) as close as possible to the respective bumps/pads. Also, place the RFIO match and WuRX match (if applicable) as close to the respective bumps/pads as possible.
    - Note: There are resistor options in the Module Board on DVDD1 (R3), VDDAUX (R7), and AVDD1P (R8) that are not required on the customer's PCB - they are reserved for internal use.

- It is recommended to route as many outer-row bumps/pads on the same layer (i.e., try avoiding via) as the ATM2251 - these particularly apply to power traces (such as LEXT1|2, VBATT, VDD1A, VDDIOP & VDDIO, DVDD1), the 16 MHz XTAL traces, and the RF traces (RFIO and WuRX (if applicable)). An example illustration is shown below in Figure 13.

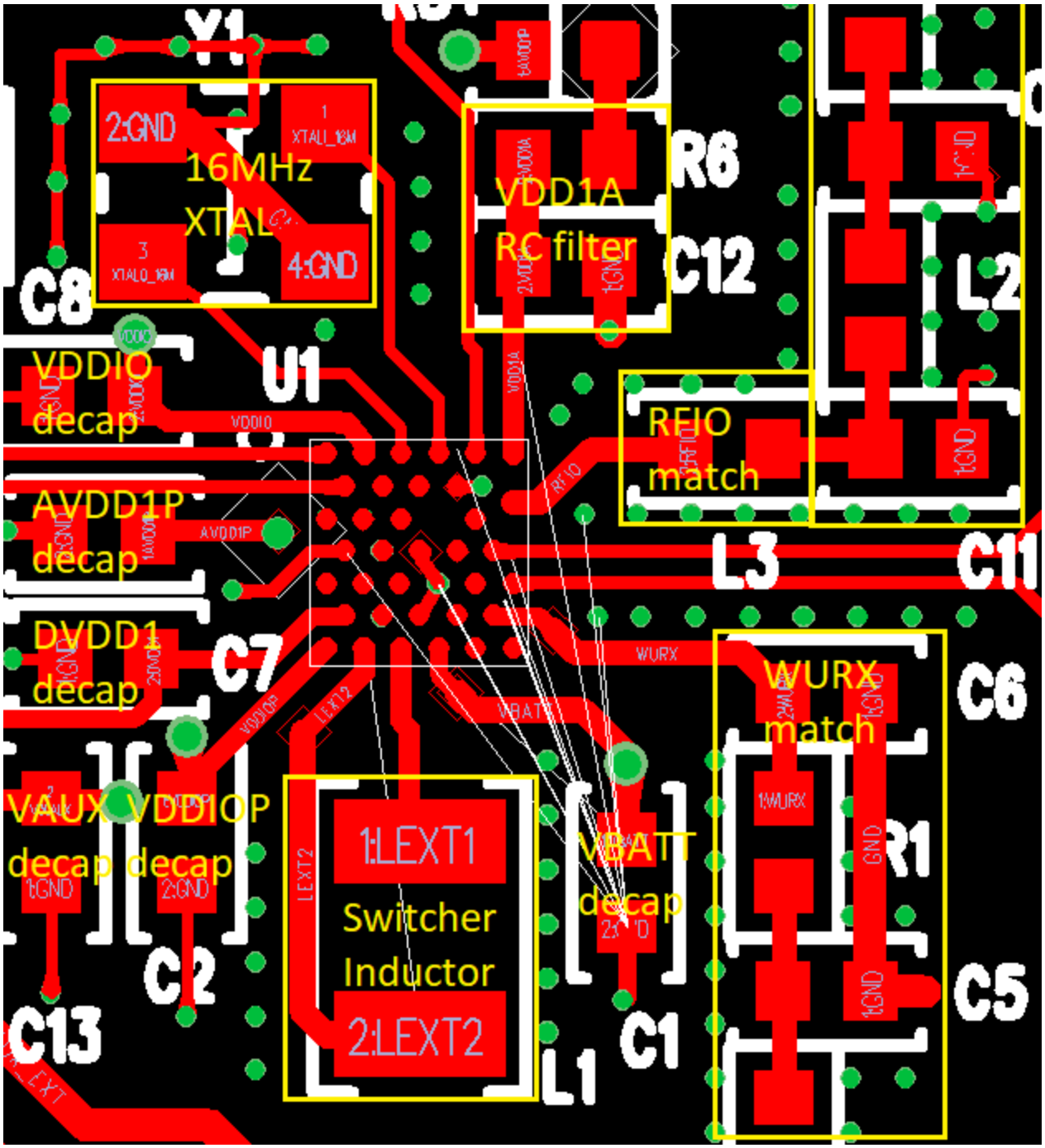

Figure 13 - Power Traces Same Layer Routing Example

- AVDD1P & VDD1A routing: Since the bump/pad is located in an inner row, the inner layer trace from the bump/pad to the 10 µF capacitor, and the remainder of the trace leading up to the R-C filter should have minimum cross-talk with other traces and a clean GND in adjacent layers. For example, in the ATM2251 EVB, the AVDD1P and VDD1A traces in

layer 4 have a clean GND in layer 5. Figure 14 below shows the routing of the AVDD1P trace (in blue) as done in the EVB PCB.

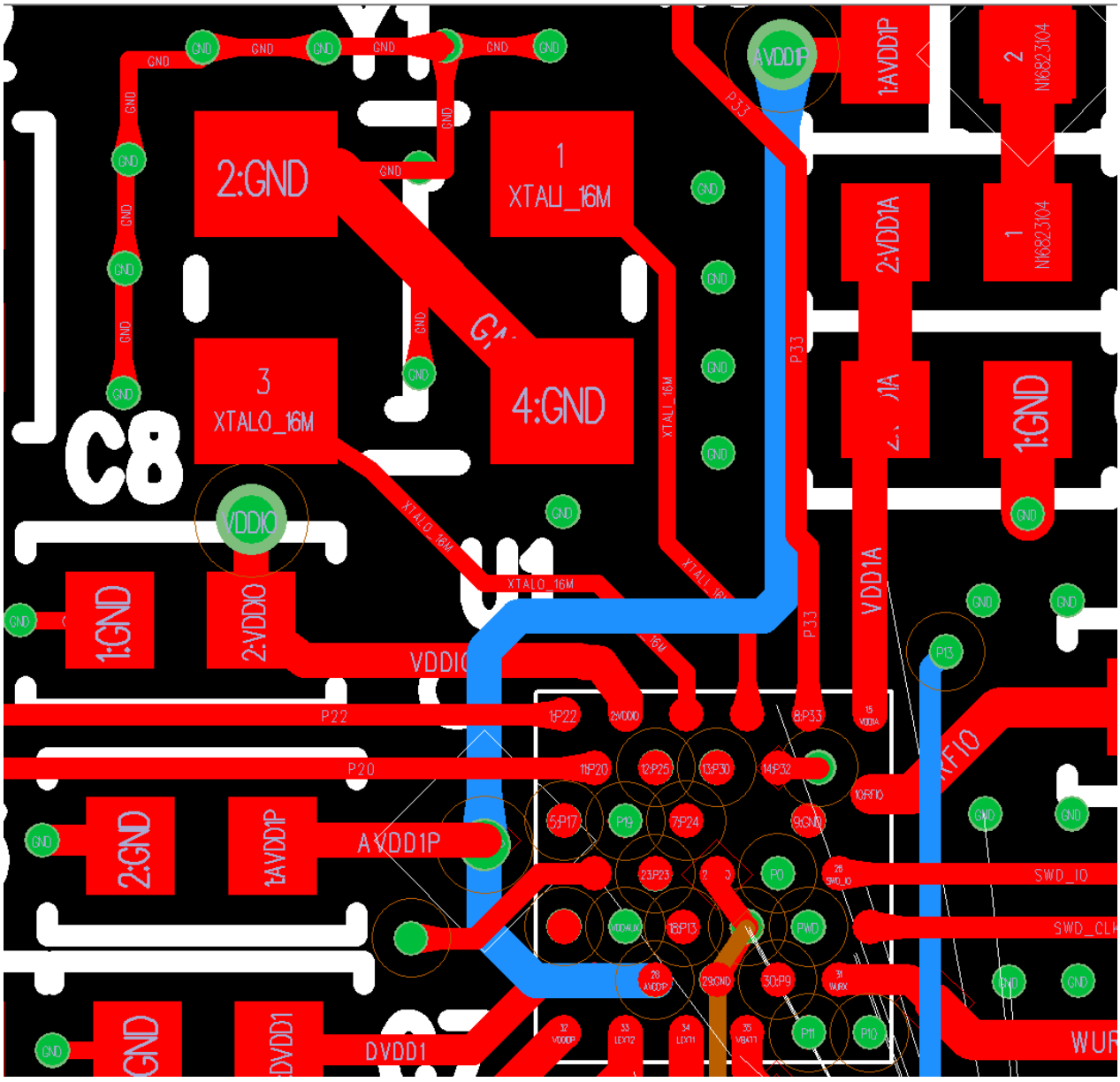

Figure 14 - AVDD1P Routing

- In the EVB, the vias in pads are filled with 4 mil drill/8 mil copper pads. The non-functional pads are, or can be, removed in inner layers - this helps with PCB fabrication. This would also allow a 3 mil drill-to-copper clearance for fanning out inner layer traces.
- There are 4 GND bumps under the package. For best results, have a Through Hole (T/H) via GND under each of these pads. If there are routing constraints in doing so, such as in

the ATM2251 EVB, it is recommended to have a T/H via under at least 3 GND pads - the GND pad near the RFIO pad, the GND pad near the switcher inductor pads (LEXT1/LEXT2), and a third GND pad near the switcher inductor GND pad. These are shown in Figure 15 below where the 3 GND vias are highlighted in bold yellow circles, and the fourth GND pad is connected with a top layer trace.

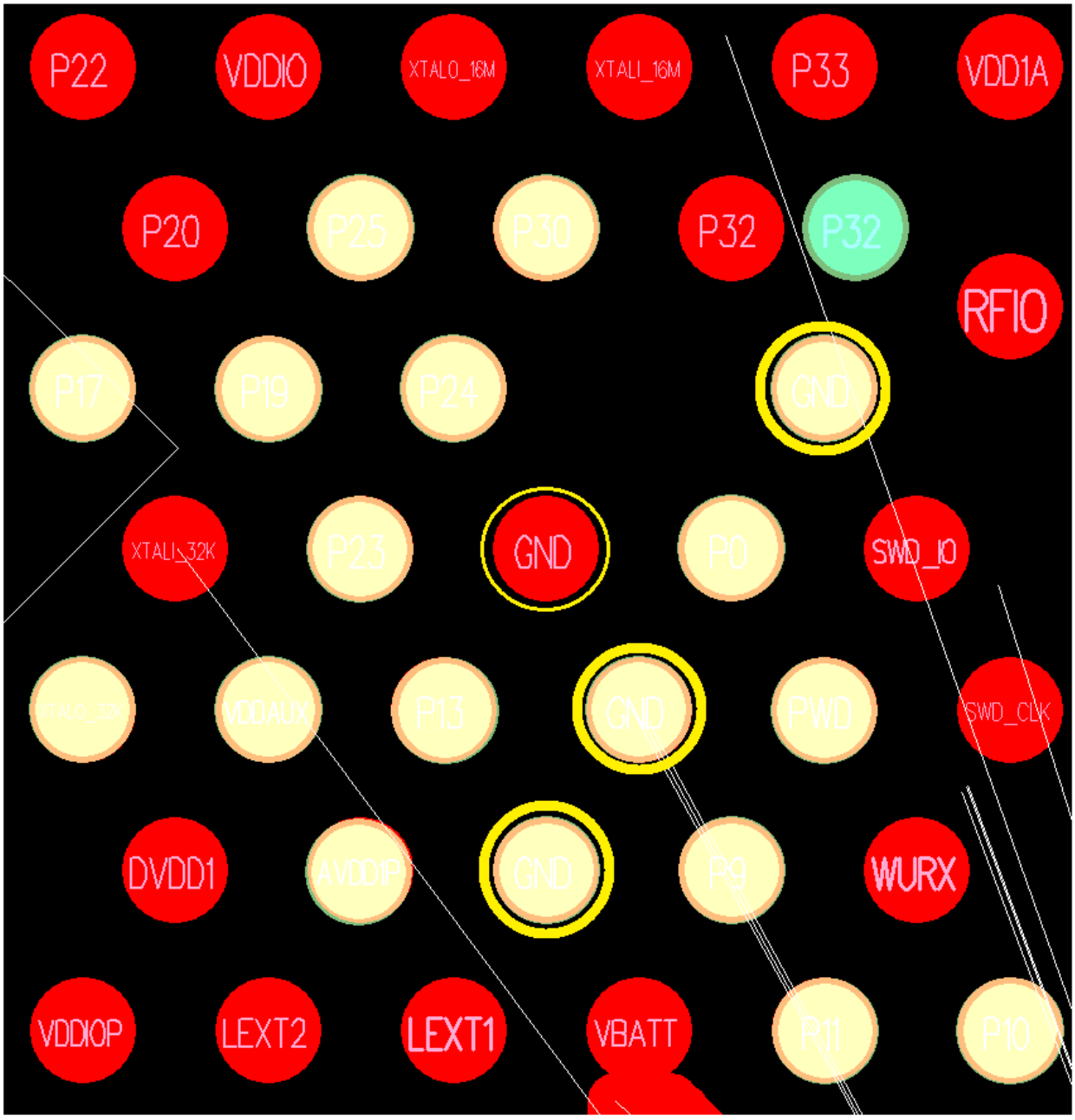

Figure 15 - Highlighted GND vias

6 Matching Guidelines

6.1 RFIO (Bluetooth LE) Section

The S11 and impedance measurements (in a powered-off state) as seen from the RFIO (Bluetooth LE) Antenna port (SMA) on the EVBs are tabulated in Table 1.

Board	S11 (dB)			Z (Ω)		
	2402 MHz	2440 MHz	2480 MHz	2402 MHz	2440 MHz	2480 MHz
ATMx20x (5x5 mm package) EVB	-15	-18	-25	62+j17	59+j10	53+j5
ATMx221 (6x6 mm package) EVB	-13	-12	-11	33+j4	30+j6	28+j9
ATM2251 (CSP package) EVB	-23	-18	-15	46-j5	40-j5	36-j5

Table 1 - S11 and Impedance Measurements from RFIO Antenna Port

As mentioned in a previous section, there are five components in the RFIO front-end section - a fourth-order (LC-LC) filter followed by a series DC blocking capacitor.

While performing the tuning on a PCB, the following parameters should be paid attention to for meeting the specifications:

- Tx output power
- Tx current
- Rx Sensitivity
- Harmonics (conducted and radiated)

6.2 Wake-up Radio Section

The impedance measurements at 2.44 GHz on the EVBs are tabulated in Table 2.

Board	Z looking into the chip (without matching circuit)	Z looking from SMA port (with matching circuit)
ATMx20x (5x5 mm package) EVB	5-j10 Ω	47-j9 Ω
ATMx221 (6x6 mm package) EVB	8+j3 Ω	34+j19 Ω
ATMx231 (7x7 mm package) EVB	5-j10 Ω	N/A
ATM2251 (CSP package) EVB	5±j5 Ω	61-j5 Ω

Table 2 - Impedance Measurements from Wakeup Radio Antenna Port

6.3 RF Harvester Section

The S11 and impedance measurements as seen from the RF Harvester Antenna port (SMA) on the EVBs are tabulated in Table 3. The measurements were made at 915 MHz at -10 dBm input power when the power rails were up.

Broad	S11 (dB)	Z (Ω)
ATMx20x (5x5 mm package) EVB	-26	55+j1
ATMx221 (6x6 mm package) EVB	-13	50-j22

Table 3 - S11 and Impedance Measurements from RF Harvester Antenna Port

ATMOSIC TECHNOLOGIES - DISCLAIMER

This product document is intended to be a general informational aid and not a substitute for any literature or labeling accompanying your purchase of the Atmosic product. Atmosic reserves the right to amend its product literature at any time without notice and for any reason, including to improve product design or function. While Atmosic strives to make its documents accurate and current, Atmosic makes no warranty or representation that the information contained in this document is completely accurate, and Atmosic hereby disclaims (i) any and all liability for any errors or inaccuracies contained in any document or in any other product literature and any damages or lost profits resulting therefrom; (ii) any and all liability and responsibility for any action you take or fail to take based on the information contained in this document; and (iii) any and all implied warranties which may attach to this document, including warranties of fitness for particular purpose, non-infringement and merchantability. Consequently, you assume all risk in your use of this document, the Atmosic product, and in any action you take or fail to take based upon the information in this document. Any statements in this document in regard to the suitability of an Atmosic product for certain types of applications are based on Atmosic's general knowledge of typical requirements in generic applications and are not binding statements about the suitability of Atmosic products for any particular application. It is your responsibility as the customer to validate that a particular Atmosic product is suitable for use in a particular application. All content in this document is proprietary, copyrighted, and owned or licensed by Atmosic, and any unauthorized use of content or trademarks contained herein is strictly prohibited.

www.atmosic.com