ATM33/e Series Hardware

Design Guide

SUMMARY: This document describes how to implement hardware designs with the ATM33/ATM33e Wireless SoC Series, including layout guidelines, RF matching guidelines, digital I/O connections and PMU (Power Management Unit) configuration.

Atmosic™

Doc. No. ATM33_e-DGHW-0058

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Acronyms and Abbreviations

Acronyms	Definition
ATM33e	ATM3330e
ATM33/e	ATM3325 ATM3330 ATM3330e
DK	Dielectric Constant
EVB	Evaluation Board
EVK	Evaluation Kit
NVM	Non-Volatile Memory
PMU	Power Management Unit
PP	Pre-preq
RAM	Random Access Memory
ROM	Read Only Memory
SoC	System-on-Chip

1. Overview

The ATM33/e Wireless SoC Series is part of a family of extreme low-power Bluetooth® 5.3 SoC devices. This Bluetooth Low Energy SoC integrates a Bluetooth 5.3 compliant radio with ARM® Cortex® M33F application processor, 128 KB RAM, 64 KB ROM, 512 KB NVM, with ARM® TrustZone® enabled security features, and state-of-the-art power management to enable maximum lifetime in battery-operated devices.

This document describes how to implement hardware designs with the devices listed in Table 1.

Table 1 also listed the EVKs applicable to this document.

EVK	SoC Part Number	SoC Package	Kit Part Number
Evaluation Kit for ATM3325	ATM3325-5DCAQK	40-pin 5x5 mm QFN	ATMEVK-3325-QK
Evaluation Kit for ATM3325 with extended storage	ATM3325-5LCAQK	40-pin 5x5 mm QFN	ATMEVK-3325-LQK
Evaluation Kit for ATM3325 WLCSP package	ATM3325-5DCACM	49L 2.65x2.47mm WLCSP	ATMEVK-3325-CM
Evaluation Kit for ATM3330	ATM3330-5DCAQN	56-pin 7x7 mm QFN	ATMEVK-3330-QN
Evaluation Kit for ATM3330e	ATM3330E-5DCAQN	56-pin 7x7 mm QFN	ATMEVK-3330e-QN

Table 1 - Applicable EVKs, SoCs and Packages

The following topics are covered:

- PMU Configuration
- I/O Connections
- Component Selection
- Layout Guidelines
- Matching Guidelines
- Production Guidelines

2. PMU Configuration

Please refer to the `PMU Configurations` section of the **ATM33/e Series Reference Manual** for configuration options. ***Note:*** *Some of these settings may require programming the SoC's OTP, ideally during the solution's manufacturing/testing stage*.

First, choose the appropriate primary power source: VBAT or VBATLI

- If VBAT is used, VBATLI is recommended to be connected to VBAT. VBAT must be between 1.1 V and 3.3 V.
- If VBATLI is used, VBAT must be connected to a bypass capacitor (10 µF). VBATLI must be between 2.7 V and 4.2 V and recommended to be greater than or equal to 3.6 V.

Next, choosing the appropriate I/O supply configuration depends on the following factors:

1) VBAT/VBATLI voltage level
    - If VBAT is between 1.1 V and 1.8 V, the I/O supply must be internally generated.
        - Connect VDDIOP to VDDIO
    - If VBAT is between 1.8 V and 3.3 V (choose one option):
        - The I/O supply is internally generated (recommended)
            - Connect VDDIOP to VDDIO
        - The I/O supply is connected to an external supply in the recommended voltage range of 1.8 V to 3.3 V, independent of VBAT value.
            - Can directly tie VDDIO to VBAT for a simple external supply case, or to another source if different requirements exist.
    - If VBATLI is used, then VDDIO must not be connected to VBAT.
        - Recommend to connect VDDIO to VDDIOP.
2) I/O voltage level of peripherals

If the ATM33/e is interfacing to peripherals (e.g. flash, sensors, etc), they must share an I/O supply.

3) Powering peripherals
The ATM33/e is able to power peripherals from its internally generated I/O supply up to an average of 50 mA. If the combined current consumption of all peripherals exceeds this value, then the I/O supply must be tied to an external supply.

***Note**: There is a 100 mW power envelope (measured at VBAT) that is inclusive of the ATM33/e needs, and thus, as an example, if an application requires more power for a higher TX output power, then the remaining power left is what can be supplied to powering peripheral devices.*

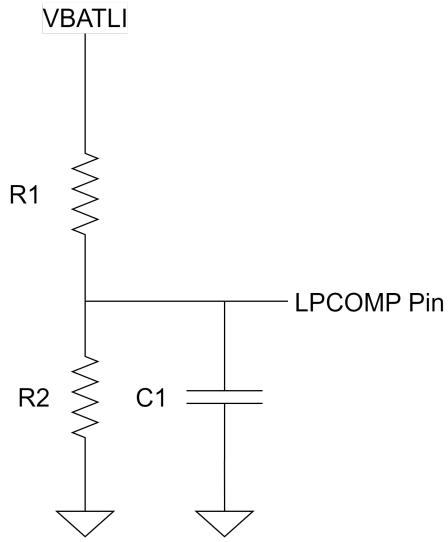
***Note:** If the application uses SoC Off, the I/O supply will not be maintained during that low power mode.*

4) External inputs
If the application uses PWD, VBAT, or VBATLI must be supplied.

- If the application uses P5 for GPIO wakeup from SoC Off, or P3/P4 for analog comparator wakeup from SoC Off.

  ***Note**: P3 does not exist on some packages. Please check the datasheet for details.*

- Example using analog comparator (also known as LPCOMP) to wake up when VBATLI crosses a threshold voltage:



R1 = R2 = 100 MΩ
C1=1 nF
LPCOMP Pin is a choice of P3 or P4

Figure 1 - Example for External Inputs

5) Must connect DVDD1P to DVDD1, with bypass capacitors of 10 µF and 1µF placed as close to the respective pins.

6) Must connect AVDD1P to AVDD1, with 10 µF bypass capacitors placed as close to the respective pins, and the series 1 Ω placed as close to the AVDD1 bypass cap as possible to be used as a low-pass filter. Please see the Analog Supply (AVDD1P & AVDD1) section for additional details on what values to use in certain situations.

7) VDDPA connection
   a) When the maximum TX output power is 4 dBm or lower, then it is recommended to connect VDDPA to ground, and a bypass cap or other connections are not necessary.

   b) When TX output power is greater than 4 dBm (6 dBm, 8 dBm, or 10 dBm), VDDPA must be connected to VDDIOP with a 1 µF bypass cap placed as close as possible to the VDDPA pin.

   c) Note that VDDPA must not be connected to a supply higher than 1.8 V. Do not connect to VAUX or any other higher supply when VDDPA is connected to VDDIOP.

   d) If the 10 dBm TX setting is used, the AVDD1 bypass capacitor needs to be increased to 22 µF. See also Analog Supply (AVDD1P & AVDD1) section for additional placement guidelines and other considerations.

e) If VDDIOP is loaded with greater than 3 mA average loads and is also connected to the VDDPA pin, the receive sensitivity may be impacted depending on the specific board layout. If this issue is seen, we recommend adding a series inductor or ferrite bead along with the VDDPA bypass cap. On the ATM33/e EVB, this issue is resolved using a 120 nH inductor in series to the bypass capacitor at VDDPA.

8) VAUX bypass capacitor must be 4.7 µF.

3. I/O Connections

All of the ATM33/e digital I/O have programmable functionality and using the Atmosic Pinmux Tool in the SDK is recommended for selecting digital I/O functionality. The following sections cover some additional considerations.

3.1 Production Test Support

The production test setup needs access to the following connections:

- VBAT or VBATLI
- GND
- PWD for resetting the DUT
- P25 for configuring the DUT to the MCU idle state
- P0 and P1 for SWD to program the DUT
- UART0 for RF testing via DTM (2-wire) or HCI (2-wire or 4-wire) interface

3.2 Connection Tips

- Power Down (PWD) should be pulled low to allow for debug and production test support. Pulses of voltage greater than 0.7V and greater than 1ms in duration are recommended when this pin is used for resetting the chip.
    - For applications that require the chip to reset when a battery connected to VBAT is replaced, a 1ms pulse can be generated from the VBAT using

the following RC topology, assuming VBAT=3 V:

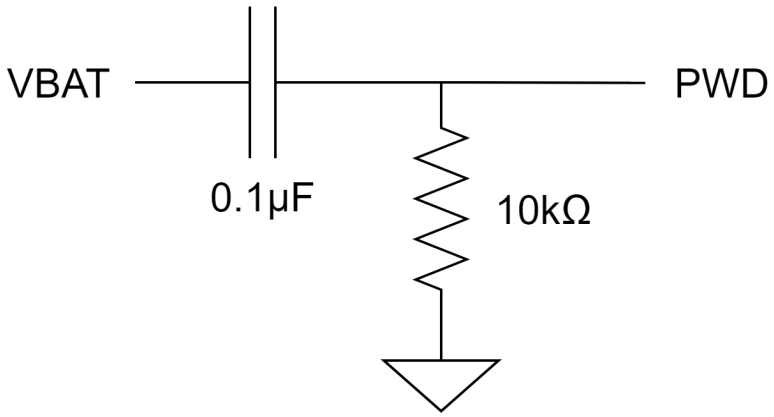


Figure 2 - Circuit to generate PWD from a battery replacement

Note that due to board parasitics, component variations, and battery characteristics (voltage, drive strength), these values may need to be tuned to achieve the required pulse voltage and duration.

- P25 requires a weak pull-down resistor and should not be tied to power or ground. P25 should be pulled low during MCUboot to allow for normal operation, debug, and production test support. If P25 is pulled high during MCUboot, the MCU will enter an idle state suitable for certain operations such as programming the on-chip NVM. After the MCU boots, P25 can be reconfigured and used as a normal GPIO. The sizing of this pull-down will depend on many factors, including post-boot configuration, and how long of a PWD pulse is needed to discharge this pin to be detected as low to boot the application, or high to enter the MCU idle state, all of which depend on the solution requirements.

- For applications that use external I/O supply, external flash, and will be operating in SoC Off or PWD modes, the flash CS#, WP#, and HOLD#/RESET# pins should be pulled up to minimize flash power consumption during those low power modes.

- All ATM33/e digital I/O have a typical drive strength of 16 mA at 1.8 V, and 48 mA at 3.3 V. As a result, some LEDs and sensors can be powered directly by ATM33/e digital I/O.

- Any ATM33/e digital I/O can be programmed to have an internal pull-up or pull-down regardless of its selected functionality. The typical resistance is 125 kΩ, independent of voltage.

***Note**: If the application uses SoC Off, the internal pull-up and pull-down will not be maintained during that low power mode.*

- The default hardware state for most ATM33/e digital I/O is high-Z. P0/P1 default state is input once the SoC is out of reset, with P0 pulled down, and P1 pulled high via internal pull-up/down resistors.

- If an external resistor divider is being used when the Application ADC is measuring an external analog signal, settling time will be affected due to the ADC's 400 pF input capacitance. For a speed of 2 Msps with 11-bit resolution, total equivalent resistance should not exceed 80 kΩ. If a transistor is being used to enable the Application ADC circuit, please ensure that the ATM33/e I/O is pulled low when the transistor is off.

- RES pins must tie to ground.

4. Component Selection

4.1 Flash

The flash used on the ATM33/e EVB is the MX25R4035FZUIL0 from Macronix. It was selected to minimize system power consumption and maximize system performance. The ATM33/e supports the following serial flash families:

Manufacturer	Part Number	ID #
Macronix	MX25Rxx	0x28c2
Gigadevice	GD25WQxx	0x65c8
Winbond	W25QxxEW	0x60ef
Giantec	GT20Qxx	0x40c4
Puya	P25QxxU	0x4085

Table 2 - Serial flash families

4.2 16 MHz Crystal

The 16 MHz crystal used on the ATM33/e EVB is the ECS-160-8-36-JTN from ECS (+/-20 ppm tolerance, +/-20 ppm stability, 8 pF load capacitance, 80 Ω maximum ESR).

This can be used as a reference when choosing alternate parts (e.g. Epson FA-20H 16.0000MF20X-AJ or Abracon ABM10W-16.0000MHZ-8-D1X-T3).

The ATM33/e supports up to +/-50 ppm total combined stability and tolerance as required by the Bluetooth 5 specification.

The ATM33/e can support load capacitance up to 12 pF with internal tuning capacitors, but < 9 pF is recommended for lower power consumption.
If an alternate part with a different load capacitance is used, the ATM33/e internal tuning capacitors may need to be adjusted. This can typically be done via lab characterization:

1) Follow instructions in the RF Test Tool User Guide (available on the Atmosic Support website) to install and run the Atmosic RF Test Tool.
2) Connect the DUT RF port to a spectrum analyzer.
3) Select the `CAL.` tab on the Atmosic RF Tool, and click the `16MXtal Cal.` button. For each iteration, check the frequency offset on the spectrum analyzer, enter the value (Hz) in the pop-up window, and click Exit. Upon completion, the characterized value between 0 and 31 will be displayed in the Atmosic RF Tool.
4) Repeat step 3 on a handful of DUTs to confirm that the characterized value is similar across multiple devices.
5) Input the characterized value into the Atmosic Production Test Tool to be programmed during DUT manufacturing.

If a TCXO is used, its output swing must be between 0 and 1 V. The output should be connected to the XTALI_16M pin, the XTALO_16M pin should be left floating, and the extclk bit in the CMSDK_PSEQ->XTAL_BITS1 register should be set.

4.3 32.768 kHz Crystal

The 32.768 kHz crystal used on the ATM33/e EVB is the SC20S-7PF20PPM from Seiko Instruments (+/-20 ppm tolerance, 7 pF load capacitance, 70 kΩ maximum ESR).

This can be used as a reference when choosing alternate parts (e.g. Micro Crystal AG CM8V-T1A-32.768KHZ-7PF-100PPM-TA-QC).

The ATM33/e supports up to +/-500 ppm total combined stability and tolerance as required by the Bluetooth 5.3 specification.

The ATM33/e can support load capacitance up to 12 pF with internal tuning capacitors, but < 9 pF is recommended for lower power consumption.

Please note that the ATM33/e requires high impedance between the XTALI_32k and XTALO_32k pins, so it is recommended to minimize the use of solder flux when mounting the crystal.

If the application does not require a crystal, the XTALI_32k pin should be grounded and the XTALO_32k pin should be left floating.

4.4 Switcher Inductor

The 3.3 µH multilayer chip power inductor used by the switcher on the ATM33/e EVB is the LQM2MPN3R3NG0L from Murata. The DC Resistance (DCR) of this inductor is 120/150 mΩ (typical/max), and the rated current is 1.2 A. If choosing an alternate part, it is recommended to have a similar DCR as this inductor and a rated current of 500 mA or higher.

4.5 RF Harvester Storage Capacitor

The ATM33/e EVBs by default have 10 µF (C2) and 47 µF (C8) storage ceramic capacitors on VSTORE. More capacitance can be added if more charge storage (up to 264 µF) is desired by installing 220uF for C8 and 22uF for both C2 and C68.

Please note that the effective capacitance of high-density ceramic capacitors typically decreases with increasingly applied DC voltage. Please consult the particular capacitor datasheet to arrive at the desired effective capacitance. For example, the Murata 1206 220 µF capacitors have an effective capacitance of approximately 90 µF at 3.0 V. Similarly, the 100 µF capacitors also have a derating of roughly 56 % at 3.0 V, thereby having a capacitance of about 55-60 µF at 3.0 V. Refer to Murata's datasheet.

Besides ceramic capacitors, supercapacitors can also be used as high-capacity storage capacitors. The following supercapacitors have been characterized with ATM3330e.

- Korchip SM3R3333 (33 mF)
- Korchip SM3R3703 (70 mF)
- ELNA DSK-3R3H334T (0.33 F)
- ELNA DSK-3R3H204T614 (0.2 F)
- Vinatech WEC 3R0105QG (1F)
- Kamcap HP-3R0-J354VYJ03 (0.35 F)

If a higher internal resistance supercapacitor is selected (ie. Korchip and ELNA supercapacitors from the list above), it is recommended to have a 220 µF ceramic capacitor connected in parallel with the supercapacitor to mitigate the voltage ripple. This filtering ceramic capacitor is necessary for systems with supercapacitors only and no battery.

If harvesting is not supported, VSTORE must be connected to the ground.

5. Layout Guidelines

This section describes layout guidelines to be followed on some key signals/routes to/from ATM33/e.

5.1 RFIO (Bluetooth LE) Section

The ATM33/e EVBs have a matching circuit as shown in Figure 3 and component values in Table 3.

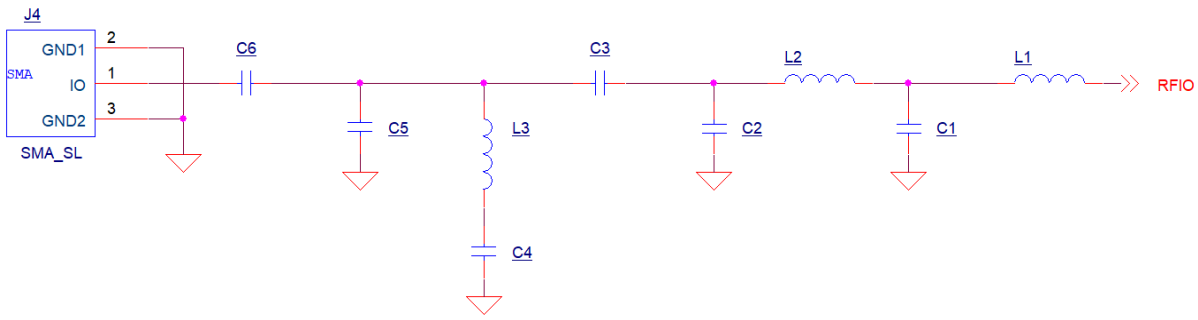


Figure 3 - RFIO (Bluetooth LE) Matching Circuit

EVB	Part Reference in Figure 1	Part Reference in EVB	Value
ATM33/e EVB	L1	L11	4.3 nH
	C1	C21	2.0 pF
	L2	L12	2.4 nH
	C2	C20	1.2 pF
	C3	C65	10 pF
	L3	L3	NL
	C4	C22	NL
	C5	C66	NL
	C6	C18	0 Ω

Table 3 - RFIO (Bluetooth LE) Matching Circuit

The two series inductors (L1 and L2) and two shunt capacitors (C1 and C2) function as a lowpass filter (assuming a pure 50 Ω termination at all harmonic frequencies) to

reject higher harmonic frequencies to meet FCC requirements. To ensure even more margin on the 5th harmonic, it is recommended that type MHQ inductors from TDK are used. If an antenna with good inherent harmonic rejection is used, this filtering network may be simplified.

The series 10 pF capacitor functions as a DC block, and can be placed at C6 or C3 depending on whether the optional notch filter L3/C4 is used and creates a DC short. C5 is a 0201 footprint placeholder intended for an ESD protection device.

An example of such a device is the ESD150-B1-W0201 from Infineon, which can significantly boost the ESD voltage protection beyond the industry standard requirement met by the ATM33/e. This optional extra protection may be used when the board is assembled in an environment where the ESD voltage exceeds that allowed by industry standards.

As for the placement of these components on the PCB, it is critical that the 4 lowpass filter components (L1, C1, L2, C2) be placed next to each other and as close to the ATM33/e as SMT assembly allows, minimizing any parasitic inductance resulting from the connecting trace, to maximize the effectiveness of the filtering and matching.

Furthermore, the current selection of the values of the filter and matching components listed in Table 3 above assumed the fixed distance between L1 and the ATM33/e on the EVB. In a layout where this distance is different, the values of the filter and matching components will need to be adjusted accordingly. L1 and C1 will be the most likely components to be adjusted to compensate for that distance.

The layout of the EVB PCB has this transmission line modeled as a Coplanar Waveguide (CPW) with a characteristic impedance of 50 Ω. The trace width/spacing can be adjusted according to the board stack-up.

If additional tuning is required, please note that the impedance of the match discussed in Table 3 when looking out from the RFIO port towards the match is roughly 25+j50 at 2.44 GHz and 5+j150 at 4.88 GHz.

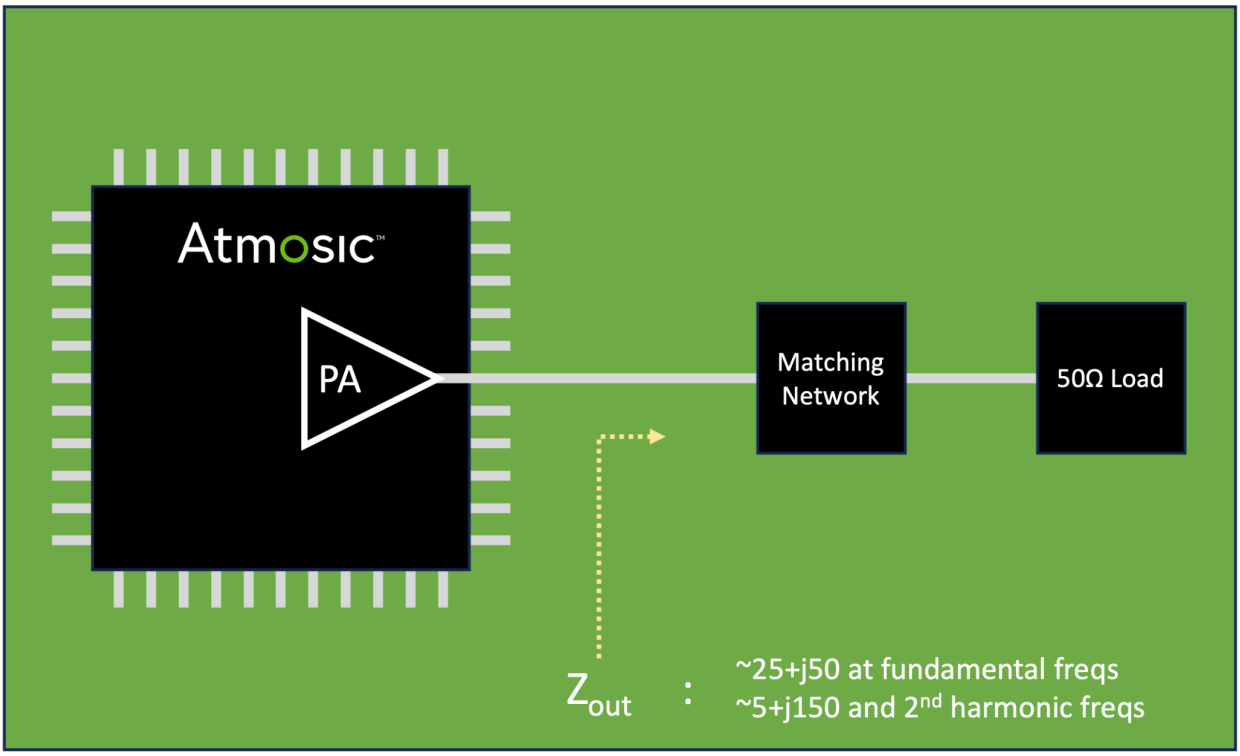


Figure 4 - RFIO Match Circuit Block Diagram

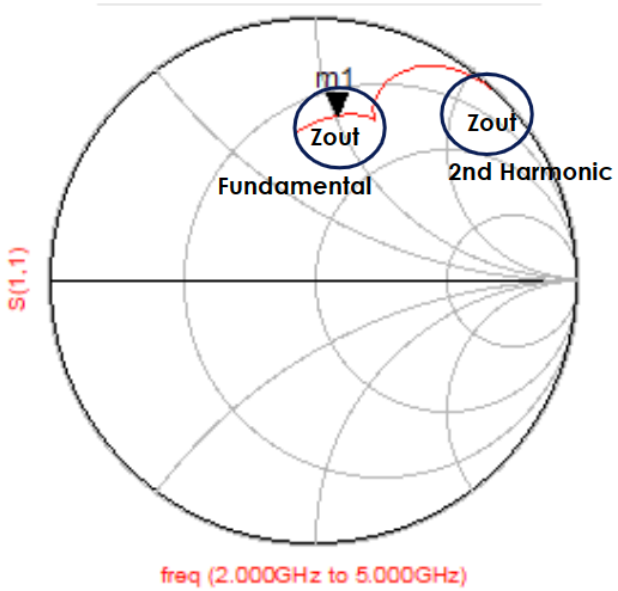


Figure 5 - RFIO Match S11 Looking Out from the SoC

For the match shown in Table 3, here is the de-embedded S11 as seen from the antenna port:

- 2402 MHz: 49 - j37
- 2440 MHz: 60.5 - j31
- 2480 MHz: 77.5 + j15

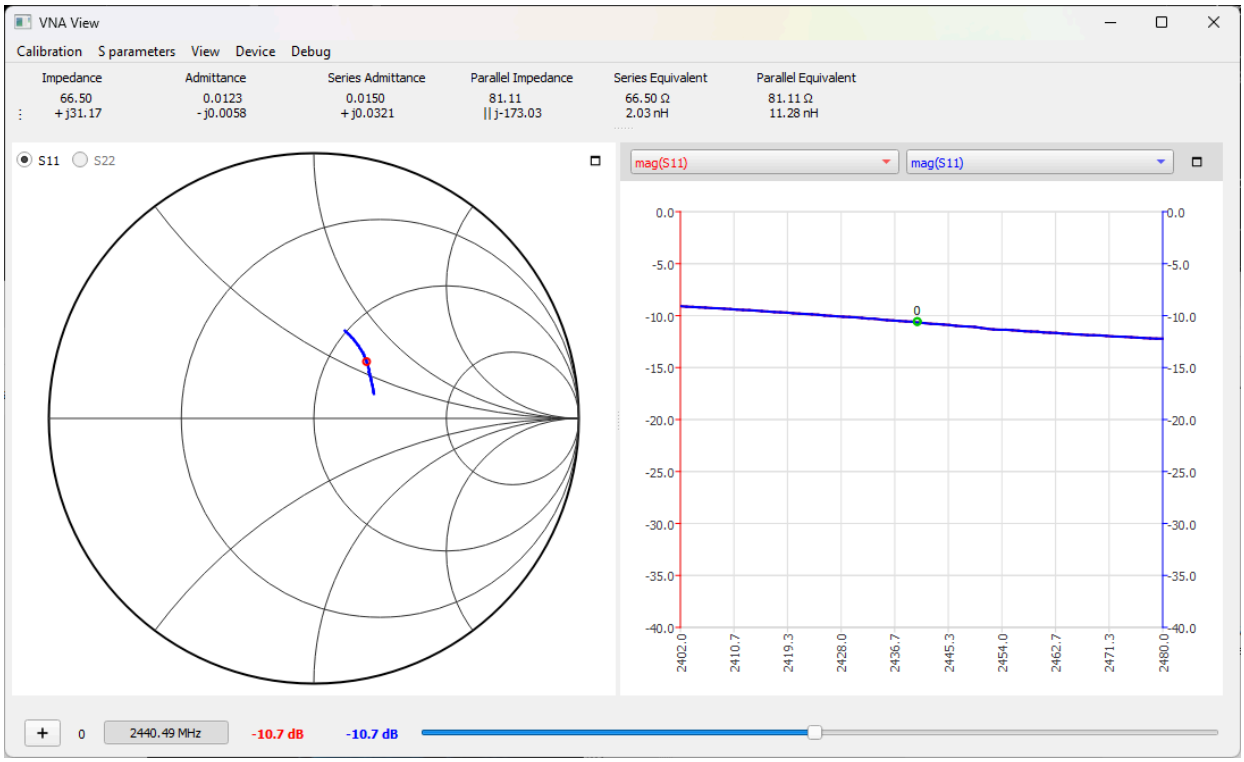


Figure 6 - De-embedded S11 of the RFIO Match Looking from the Antenna at 2440 MHz

5.2 Wakeup Radio Section

Figure 7 shows a representative matching network for the Wakeup Radio on the ATM33/e EVBs. The corresponding component values specific to 2.4 GHz and reference designators are tabulated in Table 4.

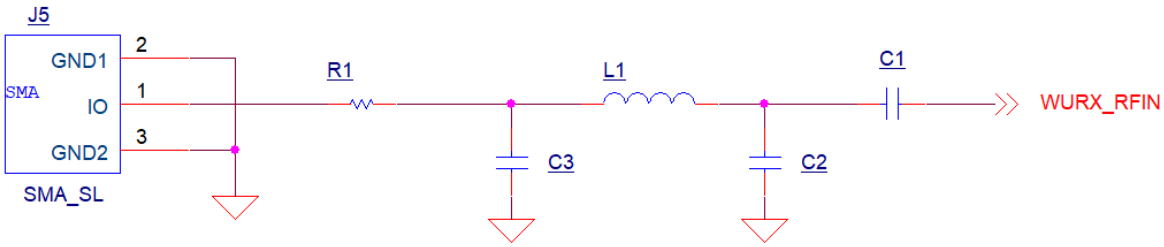


Figure 7 - Wakeup Radio Matching Circuit

EVB	Part Reference in Figure 2	Corresponding Reference Designator on the EVB	Value
ATM33/e EVB	C1	C23	10 pF
	C2	C25	1 pF
	L1	L4	2.2 nH
	C3	C24	3.3 pF
	R1	R17	0

Table 4 - Wakeup Radio Matching Circuit for 2.4 GHz

As for the placement on PCB, the components shall be placed next to each other and as close to the ATM33/e as possible.

The layout of the EVB PCB has this transmission line modeled as a CPW with a characteristic impedance of 50 Ω. The trace width/spacing can be adjusted according to the board stack-up.

For the match shown in Table 4, the de-embedded S11 as seen from the antenna port is:

- 2402 MHz: 69 - j27
- 2440 MHz: 56.5 - j6
- 2480 MHz: 48 + j13

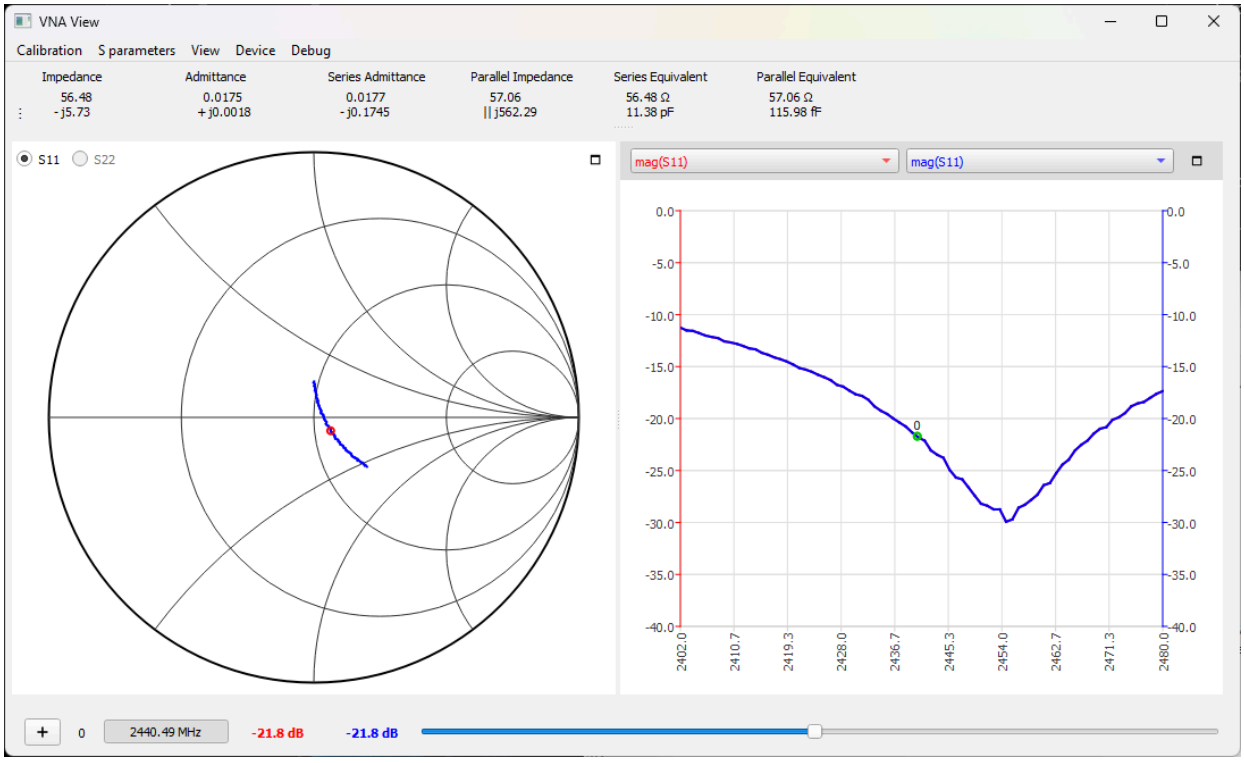


Figure 8 - De-embedded S11 of the WURX Match Looking from the Antenna at 2440 MHz

If Wakeup Radio is not used or supported, , the recommendation is to ground this pin.

5.3 RF Harvester Section

The ATM33e EVBs have a matching circuit as shown in Figure 9 and matching component values specific to 915 MHz in Table 5.

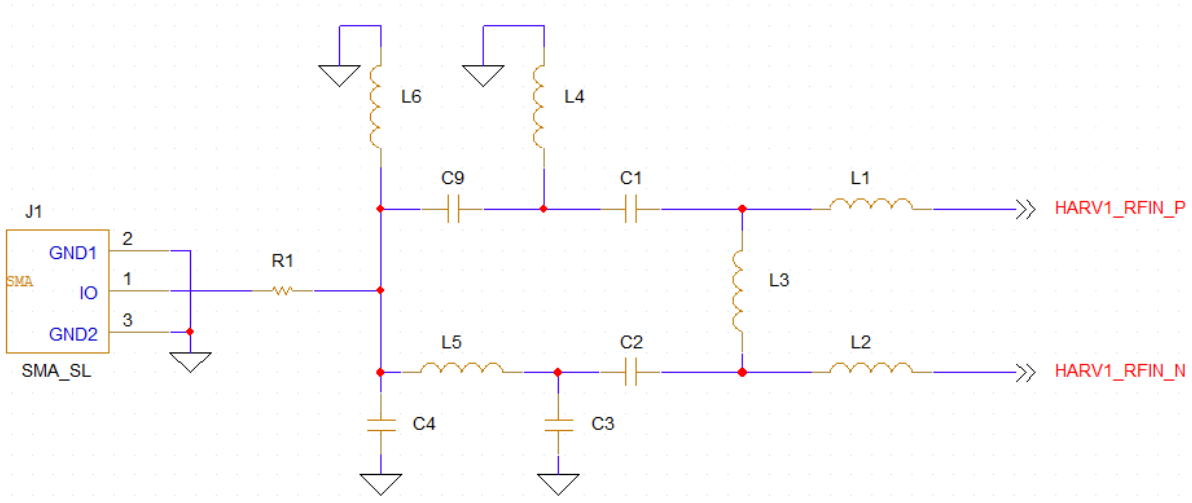


Figure 9 - RF Harvesting Matching Circuit for ATM3330e

EVB	Part Reference in Figure 2	Corresponding Reference Designator on the EVB	Value
ATM33e EVB	L1	L7	12 nH
	L2	L10	12 nH
	L3	L8	15 nH
	C1	C27	100 pF
	C2	C28	100 pF
	L4	L6	10 nH
	C3	C30	2.7 pF
	C9	C26	2.7 pF
	L5	L9	10 nH
	L6	L5	NL
	C4	C29	NL
	R1	R18	0 Ω

Table 5 - RF Harvesting Matching Circuit for ATM3330e for 915 MHz

It is recommended to follow the layout recommendations below:

- The trace from the antenna to the harvester matching circuit shall have a characteristic impedance of 50 Ω.
- As for the placement on PCB, the components shall be placed next to each other with the chip-facing component (L7/L10 in the case of EVBs) placed as close as possible to the chip pins.
- Place the 10 µF capacitor on VHARV close to the Atmosic device (pin 13 on 5x5 mm package, pin 19 on 7x7 mm package). Priority should be given to the matching components, but this capacitor should not be far from the Atmosic device pin.

For the match shown in Table 5, here is the de-embedded S11 as seen from the antenna port for 915 MHz and 2440 MHz are:

- 915MHz: 60-j26

- 2440MHz: 9.0+j0.65

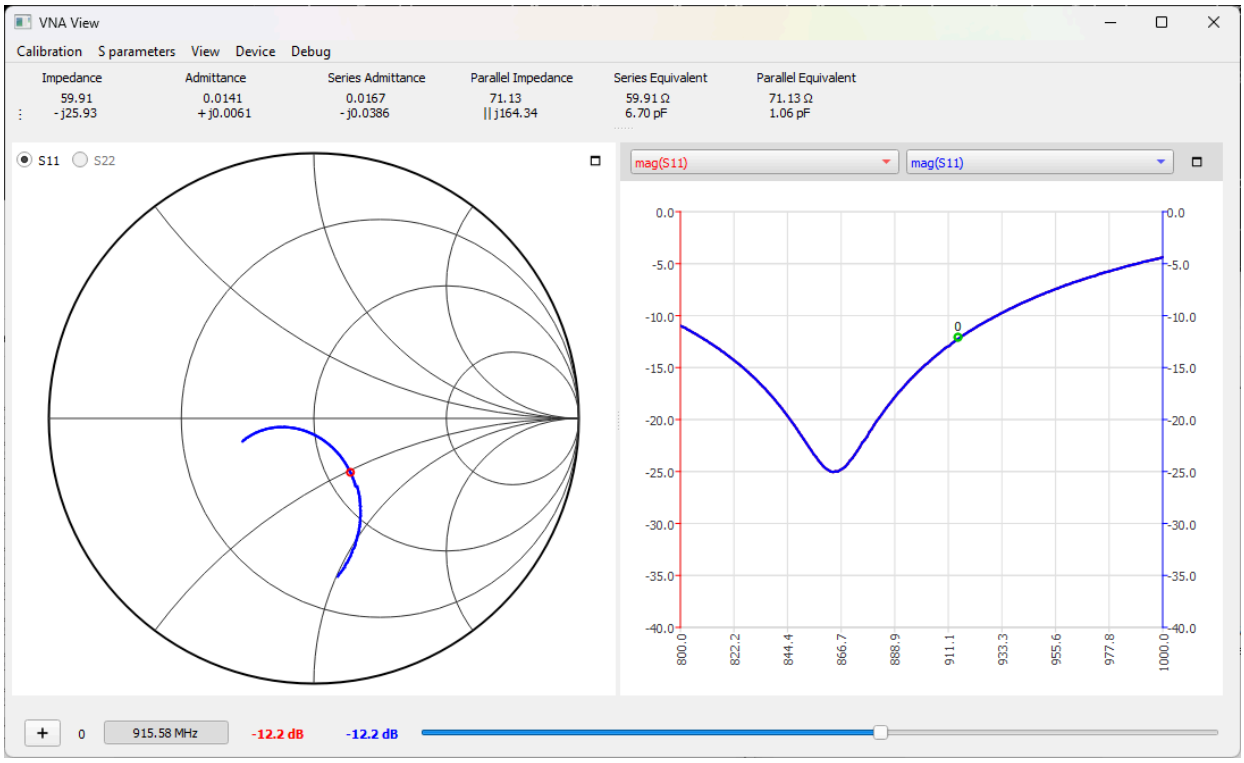


Figure 10 - De-embedded S11 of the RF Harvesting Match at 915 MHz

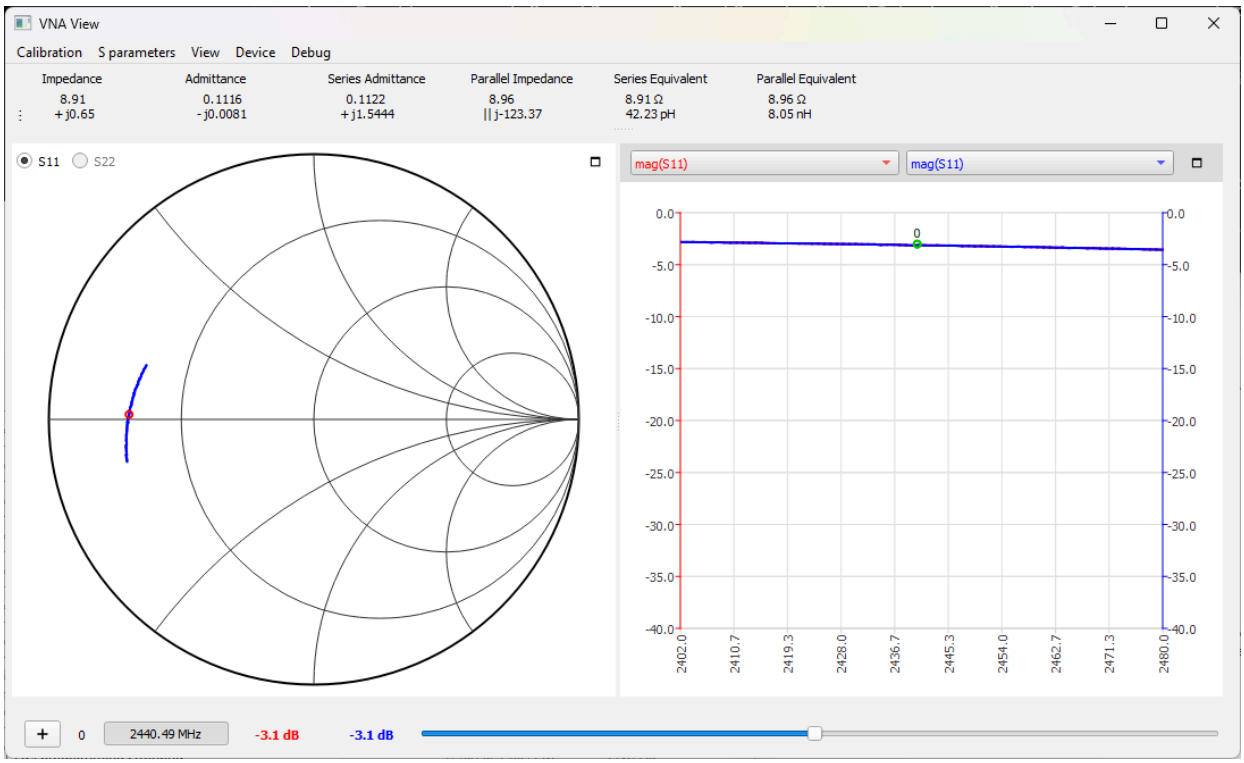


Figure 11 - De-embedded S11 of the RF Harvesting Match at 2440 MHz

5.4 Board Stack-up

While the board stack-up can be chosen according to the needs of the application, the stack-up of the current version of ATM33/e EVBs is shown in Figure 12. The board thickness is 62 mils (or, 1.58 mm).

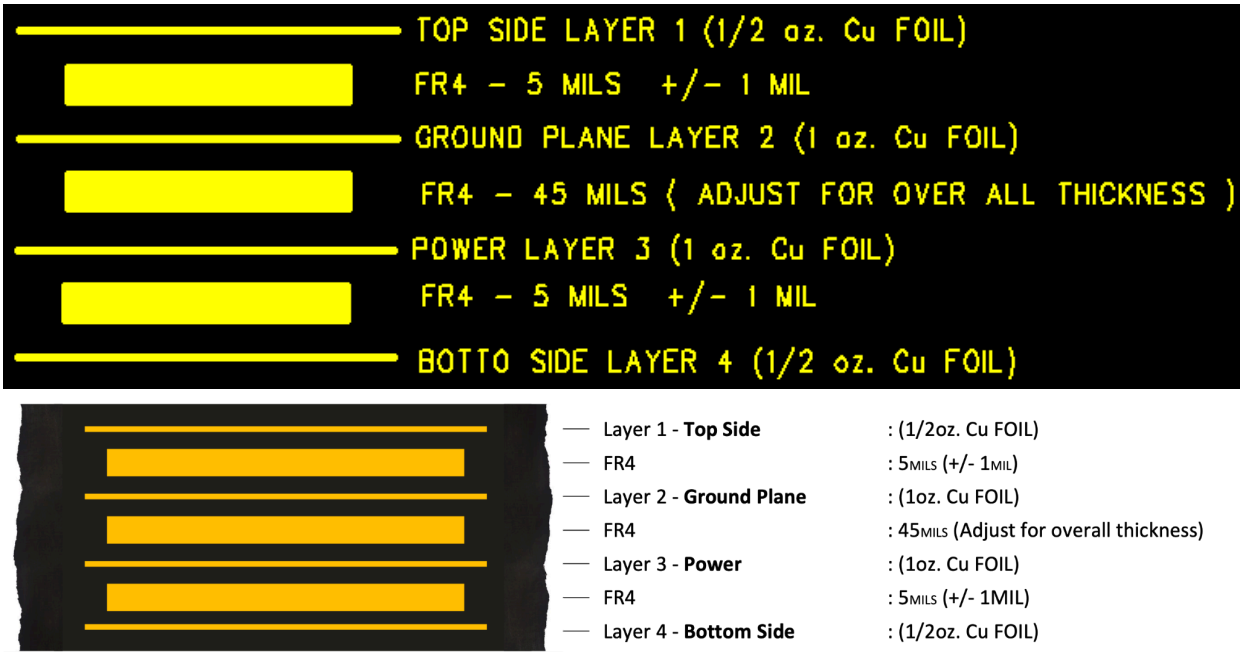


Figure 12 - Board Stack-Up

Also, shown in Figure 13 is another example of a 4-layer stack-up for thinner (32 mils/0.8 mm) PCBs.

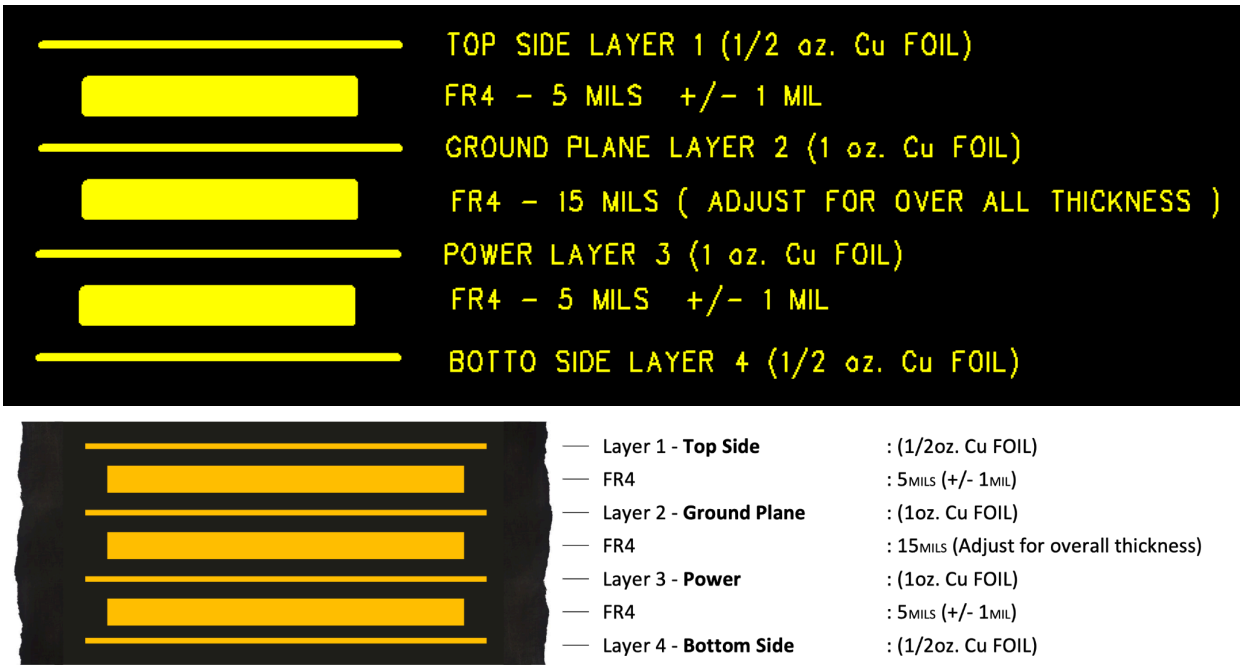


Figure 13 - 4-Layer Stack-up for Thinner PCB

5.5 Switcher Inductor

For ATM33/e 7x7 mm QFN package based 4-layer PCBs, the 3.3 µH switcher inductor needs to be placed as close as possible to pins 21 and pin 23. However, priority is given to the decoupling capacitor connected to pin 20 (VBAT), pin 24 (VDDIOP), and pin 25 (AVDD1P). A trace width of at least 10 mils is recommended and minimizes the loop area formed by the traces, inductor, and the Atmosic device. Avoid routing sensitive small analog signals on all layers beneath the inductor. Figure 14 illustrates a recommended layout for the above mentioned guideline.

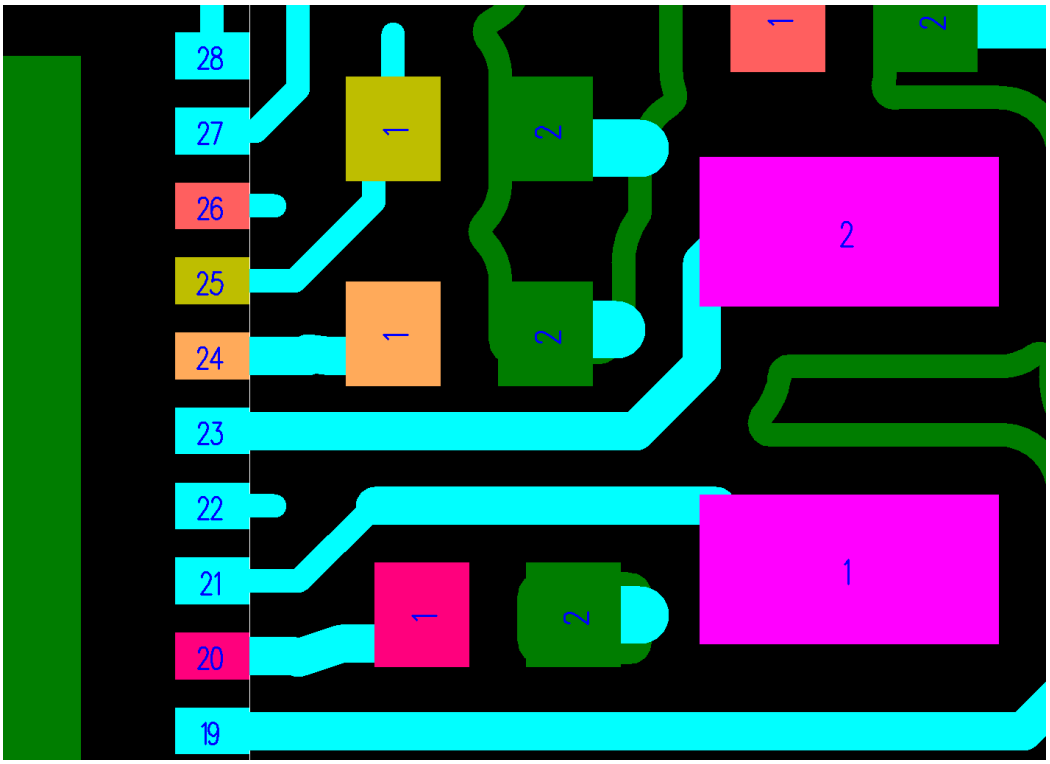


Figure 14 - Switcher Inductor Layout Recommendation for ATM33/e 7x7 mm Package PCB

For ATM3330e 5x5 mm package QFN based 4-layer PCBs, the recommendation is similar as the 7x7 mm package, but its respective pins are different for the inductor and nearby voltage rails: pins 15 and pin 17 for the inductor, and bypass capacitors close to pin 14 (VBAT), pin 18 (VDDIOP), and pin 19 (AVDD1P).

For ATM3325 5x5 mm package QFN based 4-layer PCBs, the recommendation is similar as the ATM33/e 7x7 mm package, but its respective pins are different for the inductor and nearby voltage rails: pins 14 and pin 16 for the inductor, and bypass capacitors close to pin 13 (VBAT), pin 17 (VDDIOP), and pin 18 (AVDD1P).

5.6 Analog Supply (AVDD1P & AVDD1)

The placement of bypass capacitors on the analog rail and its routing from AVDD1P pin to AVDD1 pin is critical to the performance of the PMU and radio blocks.

- Place the 10 µF bypass cap on AVDD1P as close as possible to the pin (pin 18 on ATM3325-based PCBs with 5x5 mm QFN package, or pin 19 on the ATM33e-based PCBs with 5x5 mm QFN package, or pin 25 on ATM33/e-based PCBs with 7x7 mm QFN package). This capacitor must be placed on the same layer as the ATM33/e device.
- While routing AVDD1P to AVDD1 via the RC filter, place the via closer to the AVDD1P bypass capacitor than to the pin/pad itself. In doing so, the AVDD1P pin “sees” less inductance (thus lower impedance) to the bypass capacitor than to the remaining trace.

- Place the RC filter (1 Ω +10 µF) close to the AVDD1 pin (pin 1 ATM33/e-based PCBs with 5x5 mm or 7x7 mm QFN package) to filter out effectively any noise that may get on the AVDD1P supply trace. The AVDD1 supply level should be within +/- 5% for performance and +/- 20% for functionality. Placing the capacitor < 3 mm from the AVDD1 pin should be enough to keep the parasitic inductance < 3 nH. If direction finding (AoA/AoD) is used, or 10dBm TX output power is used, or the solution will be used in cold temperatures (< -10°C), please use a 22 µF instead of the 10 µF bypass capacitor.

5.7 ATM3325 (Chip Scale Package)

The ATM3325-WLCSP will most likely require a PCB with a minimum of 4 layers to accommodate a dedicated ground layer (L2) and two layers for signal fanning and routing. The recommended PCB footprint for the ATM3325-WLCSP uses round pads of 0.2 mm (7.87 mils) diameters. In-pad vias will be needed to access the inner balls, and 10 mil diameter with 6 mil hole vias are recommended to avoid the high manufacturing costs of micro-vias, and at the same time preserving the performance and reliability. Note the maximum total PCB thickness may be limited to 1.2 mm to ensure high PCB fabrication yields. The ball-out has been designed such that it would be feasible to have all supporting components on one side of the board, with the 3.3 µH switcher inductor L1, crystals, decoupling capacitors, and RFIO match components placed optimally close to the ATM3325-WLCSP and connected without using vias to ensure optimum performance.

The same recommendations apply for the ATM3325-WLCSP regarding the placement and routing of the sensitive components and AVDD1P filtering for the AVDD1 supply.

The RFIO match topology remains the same as the other ATM33 packages, although the component values may vary slightly depending on their placement and routing constraints on the final target PCB form-factor. Fine-tuning these components should be done only after the placement and routing of all the components, including the antenna, on the final form-factor board have been fixed.

Below is the PCB stack-up of the evaluation board for the ATM3325-WLCSP:

Layer	Type	Material	Thickness		DK
Top Solder Mask			0.8	mil	
L1	Top	Copper + Plating	1.4	mil	
		PP	4.85	mil	3.98
L2	GND	Copper	1.25	mil	
		Core + PP	30.65	mil	
L3	Signal	Copper	1.25	mil	
		PP	4.85	mil	3.98
L4	Bottom	Copper + Plating	1.4	mil	
Bottom Solder Mask			0.8		
Total (mil)			47.25	mil	
Total (mm)			1.2001524	mm	

Table 6 - ATM3325-WLCSP Evaluation Board PCB Stack-up

6. Production Guidelines

6.1 I/O Connections

Please see Section 3.1 on which I/O connections are needed during production test support. These must be brought out to enable production testing and programming.

6.2 Programming OTP

Once the PMU configuration from PMU Configuration section is finalized, it is recommended to program certain OTP bits that may be needed during power on and before software boots, such as but not limited to the following settings:

- Battery Level
- Battery Type

Please see the **ATM33/e Series Reference Manual** section on OTP Memory for details on which bits are available to be programmed.

Reference Documents

Title	Document Number
ATM33e Series Datasheet	ATM33e-DS
ATM33 Series Datasheet	ATM33-DS
ATM33_e Series Evaluation Kit User Guide	ATM33_e-UGEVK
ATM33_e Series Reference Manual	ATM33_e-RM

Revision History

Date	Version	Description
November 6, 2023	0.58	Updated Table 1 - Applicable EVKs and cleaned up diagrams.
August 18, 2023	0.57	Updated PMU Configuration, item 1), 3) and 7), Connection Tips, Flash, RFIO (Bluetooth LE) Section, Wakeup Radio Section, RF Harvester Section. Added Production Guidelines,
April 3, 2023	0.56	Updated Table 1 - Applicable EVKs, SoCs and Packages, PMU Configuration, Connection Tips, RF Harvester Storage Capacitor, Table 3 - RFIO (Bluetooth LE) Matching Circuit, RFIO (Bluetooth LE) Section, Wakeup Radio Section, Switcher Inductor, Analog Supply (AVDD1P & AVDD1), ATM3325 (Chip Scale Package).
January 13, 2023	0.55	Updated I/O Connections, Connection Tips, Wakeup Radio Section,Harvester Section sections.
December 19, 2022	0.54	Updated PMU Configuration, , Connection Tips, RF Harvester Storage Capacitor, Table 3 - RFIO (Bluetooth LE) Matching Circuit, Table 4 - Wakeup Radio Matching Circuit, Table 5 - RF Harvesting Matching Circuit for ATM3330e, Switcher Inductor, Analog Supply (AVDD1P & AVDD1) section, renamed VDD1A to AVDD1.
August 16, 2022	0.53	Updated Connection tips, Flash, 32.768 kHz Crystal, RF Harvester Storage Capacitor, RFIO (Bluetooth LE) Section, Wakeup Radio Section, RF Harvester Section, Switcher Inductor, Analog Supply (AVDD1P & VDD1A) sections. Corrected typos.
May 13, 2022	0.52	Updated sections RF Harvester Section, Switcher Inductor.
May 9, 2022	0.51	Updated section RF Harvester Storage Capacitor
April 26, 2022	0.50	Initial version created

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