ATM33e Series

Extreme Low Power Bluetooth 5.3 SoC with Energy Harvesting

Datasheet

Overview

The ATM33e Wireless SoC Series is part of a family of extreme low-power Bluetooth® 5.3 system-on-chip (SoC) solutions. This Bluetooth Low Energy SoC integrates a Bluetooth 5.3 compliant radio with ARM® Cortex® M33F application processor, 128 KB Random Access Memory (RAM), 64 KB Read Only Memory (ROM), 512 KB nonvolatile memory (NVM), with ARM® TrustZone® enabled security features, and state-of-the-art power management to enable maximum lifetime in battery-operated devices.

The extremely low power ATM33e Series SoC, with a 0.85 mA radio receiver and a 2.5 mA radio transmitter power consumption, is designed to extend battery life for the Internet-of-Things (IoT) markets. Support for low duty cycle operation allows systems to run for significantly longer periods without battery replacement. In addition, this series of SoCs supports direct operation from harvested energy sources, including RF, photovoltaic, thermal, and mechanical. Innovative wake-up mechanisms are supported to provide options for further power consumption reduction.

Applications

Industrial and Enterprise

- Industrial IoT Sensors
- Remote Monitors

Healthcare

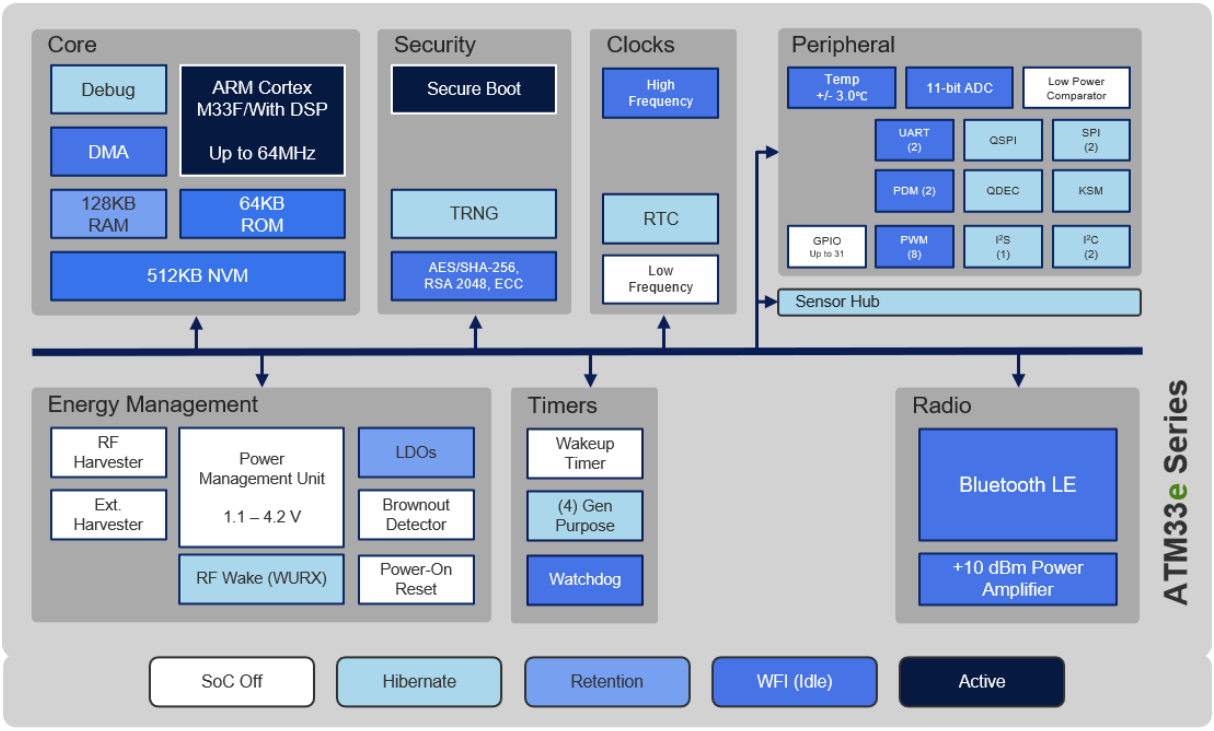
- Health Monitors
- Sports and Fitness

Home

- Advanced Home Automation
- Advanced Remote Controls
- Human Interface Devices (HID)
- Entertainment

Personal

- Gaming
- Advanced Wearables



Features

Bluetooth LE

- Bluetooth Low-Energy 5.3 compliant
- 2 Mbps, 1 Mbps 500 kbps, and 125 kbps PHY rates
- Supports Bluetooth Angle-of-arrival (AoA) and Angle-of-Departure (AoD) direction finding

MCU and Memory

- 64 MHz ARM® Cortex® M33F MCU
- 64 KB ROM, 128 KB RAM, 512 KB NVM
- Retention RAM configuration: 16 KB to 128 KB in 16 KB step sizes
- 16 MHz / Optional 32.768 kHz Crystal Oscillator

Security

- ARM® TrustZone®, HW Root of Trust, Secure Boot, Secure Execution & Debug
- AES-128/256, SHA-2/HMAC-256 Encryption/Cryptographic Hardware Accelerators
- True Random Number Generator (TRNG)

Energy Harvesting

- On-chip RF Energy Harvester
- Separate input for photovoltaic, thermal, mechanical, and other energy harvesting sources
- External energy storage interface supports a variety of storage options

RF and Power Management

- Fully integrated RF front-end
  - Rx Sensitivity: -95 dBm
  - Tx Power: +10 dBm
- Sensor Hub
- RF Wakeup Receiver
- 1.1 V to 4.2 V battery input voltage with integrated Power Management Unit (PMU)
- Radio power consumption with 3 V battery
  - Rx @ -95 dBM: 0.85 mA
  - Tx @ 0 dBm: 2.5 mA
- SoC typical power consumption with 3 V battery including PMU32 k
  - Active Rx @ -95 dBm: 1.4 mA
  - Active Tx @ 0 dBm: 3.0 mA
  - Retention @ 32 KB RAM: 1.8 µA
  - Hibernate: 1.3 µA
  - Hibernation with Wakeup Receiver: 1.6 µA

Interfaces

- I2C (2), I2S, SPI (2), UART (2), PWM (8), GPIOs (15 or 31 depending on the package option)
- Quad SPI
- 11-bit Application ADC, 4 external, 5 internal channels, up to 2 Msps
- Two mono or one stereo digital microphone input Pulse Density Modulation (PDM)
- 8 x 20 Keyboard Scan Matrix (KSM) Controller
- Quadrature Decoder (QDEC)
- SWD for interactive debugging

Package Options

- ATM3330e: 5x5 mm, 40-pin QFN (up to 15 GPIOs)
- ATM3330e: 7x7 mm, 56-pin QFN (up to 31 GPIOs)

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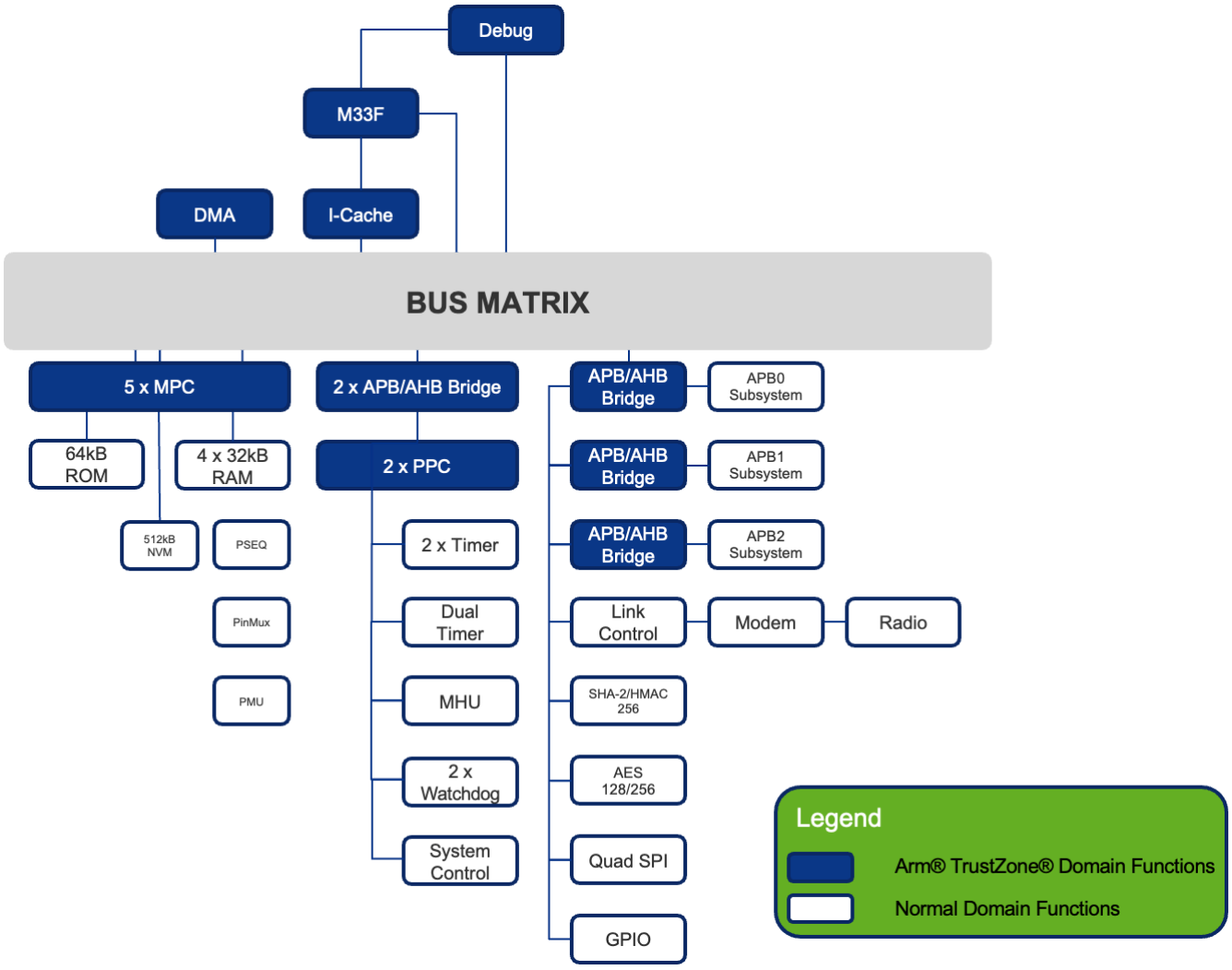


1.1 MCU & Memory

The ATM33e Series SoC contains a 64 MHz 32-bit ARM® Cortex®-M33F processor that is optimized for low-power operation. The processor is a little-endian, 32-bit RISC processor which implements the ARMv8-M architecture specification. It supports all Thumb-1/Thumb-2 instructions. It features four breakpoints, a serial access debug port, 103 interrupts, a single cycle multiplier, full wake-on-interrupt support, and two watch points. The M33F includes an IEEE-754 compliant floating point unit (FPU). The M33F also supports ARMv8-M Digital Signal Processing (DSP) extension for audio and sensor applications. The M33F core is configured with a 4 KB instruction cache to minimize instruction fetch latency.

To reduce latency, software can use the Direct Memory Access (DMA) core for memory to memory copying and for initializing blocks of memory to a constant. When it is in use, the DMA core masters the Advanced Microcontroller Bus Architecture (AMBA) High-performance Bus (AHB) and has higher precedence than the Cortex®-M33F. When interfacing to different slaves, the DMA and MCU can operate concurrently.

The ATM33e Series SoC includes the following memory components:

- ROM: 64 KB of ROM. Core elements of the firmware are placed in ROM to add security, as well as extend application space and reduce latency.
- SRAM: 128 KB of SRAM containing both system RAM and data RAM organized as eight 16 KB macros.. The power state of each macro in each low power state can be independently controlled.
- NVM: 512 KB of nonvolatile memory to store configuration, calibration data and user application and data.
- FLASH: A quad Serial Peripheral Interface (QSPI) master port to interface with an external flash chip if needed (up to 16 MB).

The quad SPI master port is equipped with a cache in the read direction to reduce the effective latency of flash accesses. The on-chip system memory is organized as follows:

Table 1.1-1 System Memory Map

Start	Stop	Block
0x0000 0000	0x0008 FFFF	ROM + NVM [Non-secure]
0x1000 0000	0x1008 FFFF	ROM + NVM (secure]
0X2000 0000	0x2001 FFFF	SRAM [Non-secure]
0x3000 0000	0x3001 FFFF	SRAM [Secure]
0x4000 0000	0x4030 4FFF	TImers, Slow 32k timer, Watchdog, GPIO, UART, PWM, SPI, KSM, QSPI/FLASH, I2C, NVM/OTP, PMU, PSEQ, SWD, GADC, Sensor Hub, PDM, I2S, DMA, SHA-2/HMAC 256 and AES-128/256 [Non-secure]
0x5000 0000	0x5030 4FFF	All of the above peripherals aliased in secure space [Secure]

Non-secure and Secure address aliases are used by the Cortex processor in secure or non-secure mode. The physical mapping of the resource (memory, peripherals) to that alias is managed by the Memory Protection Controller (MPC) and Peripheral Protection Controller (PPC). Please refer to the ***Arm® TrustZone Technology for the Arm v8-M Architecture*** manual.

1.1.1 Clocks

Primary clock domains in the ATM33e Series SoC are:

- Core clock: 32.768 kHz crystal or an internal RC oscillator (RCOSC) for low power operations
- RF clock: 8 MHz and 16 MHz fixed frequency clocks used by the link controller, modem and radio subsystem
- Backplane clock: 16, 32, 48 or 64 MHz backplane clock used by the MCU and peripherals
- PDM: 12 or 16 kHz fixed frequency PDM clock
- I2S: 16, 24 or 32 kHz fixed frequency I2S clock
- Peripherals: Additionally a subset of the peripherals can run on either the 16 MHz fixed frequency or the backplane clock

1.1.2 Reset

The Power Management Unit (PMU) releases the chip-wide reset once the power supplies have stabilized. There is no explicit reset pin on the ATM33e Series SoC but the user can use the powerdown (PWD) pin for an equivalent purpose, and when used as a reset pulse, the PWD pulse duration should be 1 ms or longer, and higher than 700 mV during the pulse duration to trigger a reset. Many of the internal modules can additionally be reset through a software register write.

1.1.3 Power Modes

The SoC supports six primary power states which are Active, WFI, Retention, Hibernation, SoC Off, and Powerdown. Each primary state may have several secondary states depending on the number of active power domains and clock gating.

1. **Active**: All regions of the SoC are powered on. Active power can be optimized by utilizing clock gating registers and/or by putting the Cortex-M33F into Wait for Interrupt (WFI).
    - Bluetooth LE Deep Sleep: Bluetooth subsystem is powered down while the remainder of the ATM33e Series SoC is powered up. This state is useful when data needs to be processed but does not need to be transmitted over RF.

2. **WFI:** When the MCU is Idle, it can be placed into WFI state to conserve power.

3. **Retention**: All or some of the 128KB SRAM, in increments of 16 KB, can be retained. All register/flip-flop states are retained. Digital I/Os will hold the state they were at when the transition into either Hibernate or Retain started. Wake can be from a timer expiring, activity detected on GPIOs, activity detected on the keyboard, activity detected on the mouse, the sensor hub reading measurements crossing a threshold, and the detection of a connection over the SWD interface. All selections about how to wake need to be programmed before the transition into the low power state is triggered. The SRAM supply voltage can be lowered to further reduce leakage power consumption.

4. **Hibernation**: Powers down system memory. Retains only a minimal amount of flip-flop state. Retains I/O state. Wake up setting must be programmed before transitioning into this state.

5. **SoC Off**: All digital domains including the top level digital domain are powered down, but the PMU remains on in an ultra low-power state with limited functionality. The system must do a complete, cold start reboot when returning from this state to an active state. Wake mechanisms are limited to

    - special 40-bit timer
    - external pin edge on P5
    - ultra-low power analog comparator with input on either P3 or P4.

6. **Powerdown** (PWD pin asserted): All power domains including the PMU are completely shut off. No supplies are internally generated or maintained.

1.2 Bluetooth LE Radio

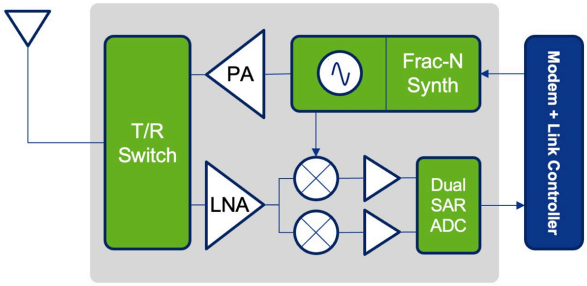
The block diagram of the low-power radio is shown in Figure 1.2-1. The radio supports 1 Mbps basic PHY, 2 Mbps high-speed PHY, 500 kbps and 125 kbps PHY. The basic 1 Mbps PHY is compatible with Bluetooth 4.0, while the 2 Mbps rate provides 2X speed and the long range rates provide up to 4X range.

The transmit path uses digital direct frequency modulation of a fractional-N synthesizer to create a constant amplitude GFSK signal that is amplified by a power amplifier to provide the desired RF output level.

On the receive path, an incoming RF signal is first amplified by an LNA before downconversion to baseband and digitized by two successive-approximation analog-to-digital converters. The digitized signal is sent to the modem for further digital processing.

The radio architecture is optimized for burst data transmission using Frequency-Hopping Spread Spectrum (FHSS) with 40 channels with 2 MHz spacing (3 advertising channels/37 data channels). Only a single RF Input/Output pin is needed, thereby simplifying board-level design. Bluetooth 5.1 AoA and AoD direction finding are supported.

Figure 1.2-1 Bluetooth LE Radio Block Diagram



1.2.1 Link Controller

The Bluetooth 5.3 link controller (LC) and host stack provides an interface between the microcontroller (MCU), modem and exchange memory, allowing the MCU to access through the AHB bus to the control registers and exchange memory.

During transmission, software writes the packet payload and control structures into the exchange memory. The link controller serializes the data into a bit stream to the modem.

During receive, the operation is reversed. Received data from the modem is processed and stored in the exchange memory to be read by software.

The design runs on an 8 MHz clock and is synchronous to the modem (16 MHz) and AHB bus (16 MHz) and exchange memory (16 MHz).

1.2.2 Modem

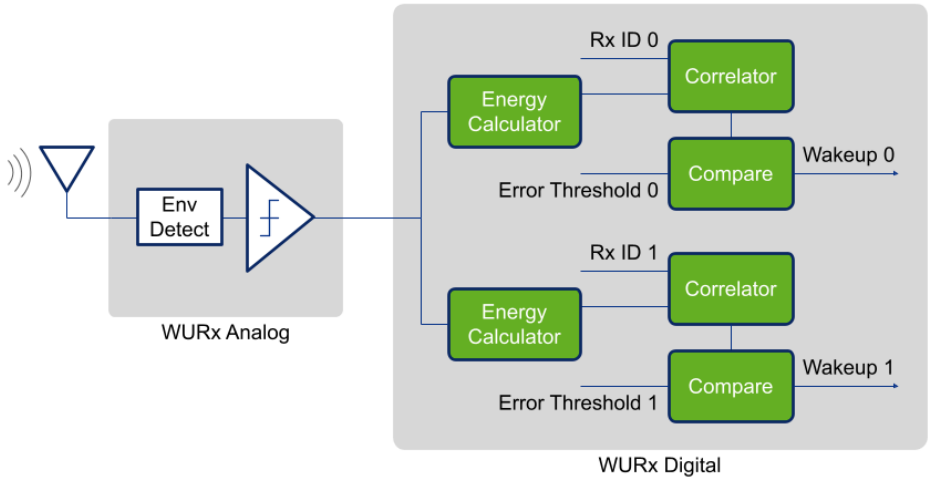
The modem, along with the radio, link controller and software stack, forms a highly efficient Bluetooth 5.3 solution. Transmission and reception support AoA and AoD direction finding and PHY rates of 2 Mbps, 1 Mbps, 500 kbps and 125 kbps are supported. The direction finding feature only supports 2 µs slots.

During receive operation, the modem and radio are enabled prior to expected packet reception as determined by the link controller. Incoming packets are detected, tracked, processed, and then forwarded to the link controller. The modem and radio receiver are turned off by the link controller at the end of a completed packet. Channel information is provided directly from the link controller to the radio without involvement of the modem.

There is minimal involvement of the modem in the transmit process. The link controller provides the symbol bit stream, which is then shaped consistent with the GFSK requirements to provide a frequency deviation for the radio. Channel information and target transmit power are provided directly from the link controller to the radio.

1.3 Wakeup Receiver

Figure 1.3-1 Wakeup Receiver Block Diagram



The use of the wakeup receiver (WURx) could further lower the power consumption. When enabled, the WURx allows the system to stay in sleep mode while listening to incoming RF signals without using the BLE radio. Only when the correct Rx ID is detected does the main radio turn on. This allows for a much lower power consumption since the WURx circuit uses very little power and much less than the BLE radio. In the case of ATM33, it uses only about 400 nA. And because the WURx is always listening, it allows for low latency. Latency of the wakeup receiver is typically in the order of 20 ms to 1 s, depending on the length of the Rx ID code used to identify the target device. Sensitivity is -55 to -60 dBm depending on the power consumption setting. WURx is intended for short range.

WURx is an OOK (On-Off Keying) receiver and uses an envelope detector to find specific patterns in the incoming signal. The best way to generate the ID is to use an OOK transmitter. The pattern of the OOK signal, will correspond to a stream of ones and zeros that the digital part of WURx would check against the Rx ID it is expecting. If transmitting a custom OOK signal isn't possible, any RF signal with the right RF frequency can be used as an OOK signal as long as its length and duty

cycle is suitable to match a reasonable ID when the envelope is sampled by a 32KHz clock. Some examples of available RF sources are iBeacon or BT inquiry. ATM33 can check for two completely different Rx IDs simultaneously. This is especially useful when listening to access points that could be either iOS or Android.

WURx is optimized to operate in the 2.4 GHz Bluetooth frequency band so that it can respond to a wakeup signal based on Bluetooth advertising packets. However, the wakeup receiver can work anywhere from 400 MHz to 2.5 GHz if the RF front end match is appropriately modified.

1.4 Power Management Unit (PMU)

The Power Management Unit (PMU) provides the core and I/O power supplies to the ATM33e Series SoC. Harvested energy can extend the battery life or enable operation without a battery for some low duty-cycle applications.

PMU generates the three power supply outputs: DVDD1P, AVDD1P, VDDIOP, and a fourth auxiliary supply VAUX used internally by the PMU. The following connections must be made on the board:

- DVDD1P to DVDD1
- AVDD1P to AVDD1

Table 1.4-1 PMU External Pins

Pin	Description
VBAT	Battery input Battery voltages from 1.1 V to 3.3 V can be used. Must connect to a 10 µF capacitor if VBATLI is used.
VBATLI	Lithium ion battery input in place of VBAT 2.7 to 4.2 V lithium ion battery supply. If lithium ion battery is not used, it is recommended to connect this pin to VBAT.
VDDPA	PA power supply
VSTORE	Connection to a large storage capacitor (typical value 220 µF). Must be grounded when the harvester is not used.
VHARV	Connection to a storage capacitor of typical value 10 µF. Must be grounded when the harvester is not used.
LEXT1, LEXT2	Terminals between which the switching regulator inductor is connected.
DVDD1P, AVDD1P VDDIOP	DVDD1P and AVDD1P are PMU generated digital and analog core supply outputs. VDDIOP is a PMU generated 1.8 V I/O supply output.

Pin	Description
VAUX	Auxiliary supply output of typical value 3.2 V, used internally by the PMU.
DVDD1, AVDD1	Power supply input for digital and analog core circuits.
VDDIO	Power supply input for digital and analog I/O circuits.

The PMU provides a brownout feature, via multiple interrupts and programmable thresholds, to help enable more reliable operation, especially when using energy harvesting.

1.4.1 PMU Configurations

The PMU must be configured correctly to ensure correct operation. The following modes of operation are supported by the PMU:

PMU Configuration	VBAT Connection	VBATLI Connection	VDDIO Connection
Battery or external power supply (1.1 V-3.3 V) with internally generated I/O supply	Battery or power supply	VBAT	VDDIOP
Battery or external power supply (1.8 V-3.3 V) with externally generated I/O supply	Battery or power supply	VBAT	VBAT or other externally generated I/O supply that is between 1.8V-3.3V.
High Voltage battery or power source (2.7 V-4.2 V) with internally generated I/O supply	Unconnected (keep bypass capacitor connected)	High voltage battery or power source	VDDIOP

1.5 Security

The ATM33e Series SoC offers a complete security solution including:

- Secure boot
- Secure Firmware Update
- Secure execution
- Key management
- Key storage
- Secure debugging

The ATM33e Series SoC has a true random number generator (TRNG) which generates a single 32 bit random number per invocation. Arbitrarily long random numbers can be achieved by repeatedly invoking this random number generator. The TRNG can also be used to seed the hash function.

The ATM33e Series SoC also has two hardware cryptographic accelerators, AES-128/256 and SHA-2/HMAC 256 which are both accessible by software. There are provisions to load keys into the AES-128/256 where the keys themselves are not readable by any bus master.

1.6 Sensor Hub

The sensor hub is operational while the rest of the SoC is in hibernation. The sensor hub can be programmed to collect sensor data via SPI or I2C and store them to the external Flash or a region in RAM periodically until the total collected data reaches a predetermined amount. SoC can then wake up and transmit the data via Bluetooth. In addition, the core can be programmed to manage the link controller to send simple Bluetooth LE advertisements in timer-based periodicity.

1.7 OTP Access

The 64-bit one time programmable memory (OTP) is used to store PMU battery configurations during the start up process. The OTP is accessible through the Advanced Peripheral Bus (APB) once the MCU is up and running and provides indirect access for byte reads and bit writes.

VAUX will need to be set to the 2.5 V setting before OTP bits are written. Reads can happen at any voltage.

1.8 Timers and Interrupts

1.8.1 Wakeup Timer

Wakeup timer is a 40-bit timer based on the low power 32 kHz clock. When this timer is enabled during SoC Off mode, it will determine the SoC off duration.

1.8.2 General Purpose Timers

There are four (4) general purpose timer cores: Timer0, Timer1, Dual Timer, and Slow Timer. The values of the timers are readable by the MCU. All timers are clocked by the medium power clock except for the Slow Timer which uses the low power clock. All these timers stop when the system enters a low power mode. The state of the timer is maintained during Retention mode but is reset during hibernate mode.

- Timer0, if enabled, will decrement from a 32 bit reload value to 0 triggering a maskable interrupt as it transitions from 1 to 0. The reload value is loaded as the next timer value when the timer reaches 0.
- Timer1 is identical to Timer0 with its own register space and its own interrupt
- Dual Timer contains two timers and each timer is independent of the other but sharing a single interrupt output. Each timer counts down and can run in one-shot, periodic, or free running mode. The timers are configurable to be either 16 bit or 32 bit. Additionally there is a prescaler in front of each timer that can reduce the incoming clock by 1x (no change), 16x, or 256x.
- Slow Timer is a 40 bit count down timer with three programmable thresholds. The interrupt is optionally asserted when the counter counts from one above the threshold to the threshold. It is recommended that the timer be read twice and the value used only if the values from both reads are the same. If the values are not the same then

the read should happen a third time. The timer is updated 16000000/32768 cycles or approximately 488 cycles of the 16 MHz medium power clock.

1.8.3 Interrupts

The SoC supports the following categories of interrupts:

- Interrupts for ARM MCU exceptions, watchdog timers, and hardware protection blocks.
- Maskable Interrupts for Peripherals:
  - 28 interrupts for APB peripherals
  - 4 DMA interrupts
  - 12 Bluetooth LE interrupts
  - 1 power sequencer interrupt
  - 31 GPIO interrupts (ATM3330e 56-pin QFN, 7x7mm), 15 GPIO interrupts (ATM3330e 40-pin QFN, 5x5mm)

1.9 Peripherals and I/O

The following peripherals are supported by the SoC.

- **GPIO**
  There are up to 31 GPIOs available on the ATM33e Series SoC 7x7 package, and up to 15 GPIOs in the 5x5 package. GPIOs are controlled through software accessible registers. In addition to drive, sample, pull up and pull down functions, the GPIOs can also be used to generate interrupts and to wake the ATM33e Series SoC from low power states.
- **I2C**
  There are two identical I2C cores that support master mode. In master mode, software preloads the transaction and then initiates the hardware controller. Software can either poll for completion or respond to the completion interrupt. I2C clock speed is programmable to specific rates between 3.9 kHz to 2 MHz. The I2C cores do not support clock stretching.
- **Serial Peripheral Interface (SPI)**
  There are two identical SPI master and slave cores. In master mode, software can preload the transaction, initiate it, and then either poll for completion or respond to the completion interrupt. Opcode, transaction type, data, and number of bytes are all software programmable. The hardware will serialize and sample incoming data as required by the protocol. The SPI port clock frequency is programmable to specific rates between 7.8 kHz to 8 MHz. One SPI core in slave mode can wake up the SoC from a low power state.
- **Quad Serial Peripheral Interface (QSPI)** supports external flash up to 32 MHz
  There is one quad SPI master port and it is intended to be connected to an external flash (if needed). Internally there are three cores that can act as master for the interface:
  (a) 1-bit core identical to the SPI core described previously. It provides read and write support to the external flash via indirect addressing.
  (b) Software specified protocol / content. The hardware's role is limited to serial shift in or out. Read and write access via indirect addressing is provided by this core.
  (c) Direct memory mapping of the entire external flash contents. It essentially acts as an AHB bridge to the

external flash. The hardware handles all protocols. Additionally this core contains a cache in the read direction to reduce latency.

- **UART**
  There are two UART cores with flow control present on the ATM33e Series SoC. UART0 should be used for HCI type applications and UART1 primarily for debug messaging (without flow control).

- **PDM**
  The PDM provides digital microphone support with programmable clock rates from 500 kHz to 4 MHz. It supports a stereo mode with left and right channels multiplexed on the same data line with the rising and falling edges of the clock. The PDM-to-PCM conversion takes a 1-bit PDM output from a digital microphone as input, and outputs a PCM signal with programmable bit width of 16/20/24-bit. The PCM sample rate is programmable (6/8/12/16 kHz) with programmable filter BWs. The low pass filtering for these provides an out-of-band attenuation of 60 dB. Additional sample rates of 24, 32, 48 and 64 kHz are available with limited filtering. The IIR filter in the signal path, which attenuates any residual DC content, has programmable order (1st, 2nd or 3rd) and bandwidth (10 Hz to 2 kHz). There is a digital gain control block with programmable gain from -30 dB to 30 dB in steps of 0.5 dB.

  The output from the PDM-to-PCM core is captured in FIFO. There are two separate sets of FIFO arrays for APB, and AHB (faster) access:

  1. APB 16-entry FIFO which overruns if not drained quickly.
  2. AHB FIFO supports a 64 x 32 ping-pong buffer. 64 entries are split into 4 arrays, bufferA to bufferD. PDM outputs are written starting at bufferA. Each entry is 32-bit which can be two 16-bit audio samples or single 20/24-bit samples with options for packing and swapping samples. AHB access is faster and data can be transferred into SRAM or NVM using direct memory access (DMA) based on application.

- **I2S**
  I2S is designed to support inter-IC sound bus for transporting digital audio data streams.
  This interface consists of:
  - SCK - system clock or bit clock or serial clock
  - WS - word select or frame clock or left/right clock
  - SD - serial data or data line

  Depending on how the module is configured as transmitter or receiver and as master or slave, the module sources or sinks these interface signals based on the configuration. Supported operation modes are PCM mode, left-justified mode and right-justified mode.

- **PWM**
  The PWM has eight independent pulse width modulation output channels. Each channel can operate in one of four modes:
  1. Continuous mode - The user specifies the duty cycle and the PWM channel outputs perpetuity.

  2. Counting mode - The user specifies the number of times to repeat in addition to duty cycle. This combination of duty cycle and repeat count is referred to as a frame.

  3. IR mode - The PWM channel outputs one frame type and, immediately on completion of the first frame, outputs a second frame. This second frame can be identical to the first or it can be different if a different set of parameters were loaded in while the first frame was going out.

  4. IR FIFO mode - The PWM core pulls the next frame information from a FIFO. One FIFO buffer is time-shared among all eight channels, therefore IR FIFO mode is only supported in the channel equipped with the FIFO buffer.

All channels support all modes of operation.

PWM frequency ranges from 122 Hz to 8 MHz with 16 bit fields to independently control high duration and low duration.

- **Quadrature Decoder (QDEC)**
  The QDEC is a 3-axis (x,y,z) quadrature decoder. Each axis is independent and requires 2 input pins. QDEC continuously updates the internal integrators and their values can be read by software.

- **Keyboard Scan Matrix (KSM) Controller**
  The KSM is a keyboard scanner which supports up to 8 rows by 20 columns or 20 rows by 8 columns. Key pressed and key released events can optionally require that the key be pressed or be released across multiple consecutive scans. Up to 12 simultaneous key events can be tracked.
  A portion of the KSM can continue to scan during low power states. The key pressed or key released event can also optionally wake the ATM33e Series SoC from a low power state. Key events are not lost when the ATM33e Series SoC is in a low power state. Key events are packetized and written into a FIFO via the hardware for later reading by the software. KSM controller pins can be reverted to GPIO if KSM features are not used.

- **Analog Comparator**
  A 16-level analog comparator provides an ultra-low power approach to sense an analog input signal from sensors.

- **Application ADC**
  11-bit Application ADC, also known as General-purpose ADC (GADC), with 4 external channels (can be configured as two differential channels, four single-ended channels or a combination of one differential channel with two single-ended channels), and 5 internal channels (battery, energy storage element, core supply, temperature, Li-ion battery). The sample rate is 2 Msps, divided when multiple channels are used.

1.10 Pin Multiplexing

The 7x7 mm, 56-pin QFN package SoC, the 31 programmable I/O pins, P0 - P30, may be connected to multiple functional signals. The 5x5 mm, 40-pin QFN package supports 15 programmable pins.

In addition, each of these I/O pins can be configured to be input only, output only, input/output, with or without pull-up. A pin multiplexing tool provided in the SDK can be used to program the I/Os to the desired function

2 Electrical Specification

All parameters' typical values are based on 3 V supply at 25 °C unless otherwise specified, and if applicable and specified, min/max values are based on the worst case process variation, voltage, and ambient temperature conditions. Radio parameters are measured using a conducted configuration.

Table 2-1 Maximum Electrical Ratings

Symbol	Parameter	Min	Typ	Max	Unit
VBAT	Battery voltage	-0.2		3.6	V
	Voltage Ramp Rate	0.01			V/ms
VBATLI	Lithium-ion battery supply	2.4		4.6	V
	Voltage ramp rate	0.01			V/ms
AVDD1	Analog core voltage	-0.2		1.3	V
DVDD1	Digital core voltage	-0.2		1.3	V
VDDPA	PA supply	-0.2		3.6	V
VSTORE	Storage element	-0.2		3.6	V
VDDIO	I/O supply	-0.2		3.6	V
VAUX	PMU Auxiliary Supply	-0.2		3.6	V
VIO	I/O pin (VDDIO > 3.4 V) I/O pin (VDDIO <= 3.4 V)	-0.2 -0.2		3.6 VDDIO+0.2	V
VRF	RF I/O pin DC Voltage			10 1.8	dBm V
VRFIN	WURX RF IN pin			-10	dBm
ESD_{HBM}	ESD HBM			2000	V
ESD_{CDM}	ESD CDM			500	V
T_{STORE}	Storage Temperature	-40		125	°C

Table 2-2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_j	Junction Temperature			125	°C
VDDIO[1]	I/O supply	1.65	1.8	3.3	V
VBAT[2]	Battery supply	1.1		3.3	V
VBATLI	Lithium-ion battery supply	2.7		4.2	V
VDDPA	PA supply	1.0	1.8	1.89	V
VSTORE	Storage element			3.3	V
VAUX	PMU Auxiliary Supply	2.5	3.3	3.3	V
VIO	I/O pin	0		VDDIO+0.2	V
	Crystal (Tolerance + Stability) - 16.000 MHz	-50		50	ppm
	Crystal (Tolerance + Stability) - 32.768 kHz	-500		500	ppm
TA	Operating (Ambient) Temperature	-40	25	85	°C

[1] VDDIO: Refer to the ATM33/e Series Reference Manual 'PMU Configurations' section for valid configurations in conjunction with VBAT/VBATLI.

[2] VBAT: Refer to the Battery Level section of the ATM33/e Series Reference Manual 'PMU Configurations' section for OTP or register settings that may limit this range.

Table 2-3 Radio Transceiver Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Supported PHY Rate	1M uncoded		1M		bps
	2M uncoded		2M		bps
	500k coded		500k		bps
	125k coded		125k		bps
Frequency	2MHz channel spacing	2.402		2.480	GHz
Rx sensitivity	37-byte packets, clean Tx				
RFPHY/RCV/BV-01-C, PER=30%	125 kbps		-101		dBm
	500 kbps		-98		dBm
	1 Mbps		-95		dBm
	2 Mbps		-92		dBm
	255-byte packets, dirty Tx				
	125 kbps		-100		dBm
	500 kbps		-96		dBm
	1 Mbps		-93		dBm
	2 Mbps		-90		dBm
Tx output power RFPHY/TRM/BV-01-C	Typical levels: 10,8,6,4,2,0,-2,-4,-6,-8,-10,-20	-20		10	dBm
Tx power accuracy			+/-1.5		dB
Tx spectral mask 1M PHY RFPHY/TRM/BV-03-C	2 MHz offset > 3 MHz offset	-20 -30			dBm dBm
Rx Carrier-to-Interferer (Bluetooth LE 1M PHY) RFPHY/RCV/BV-03-C	Co-channel interference Adjacent 1 MHz interference Adjacent 2 MHz interference Adjacent 3 MHz interference	21 15 -17 -27			dB dB dB dB
RSSI resolution			1		dB
RSSI accuracy	-90 to -20 dBm		+/-2		dB

Table 2-4 Wakeup Receiver Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity[1]	2440 MHz, 14-byte packets at 1 ms interval for 40 ms		-54		dBm
	900 MHz, 14-byte packets at 1 ms interval for 40 ms		-58		dBm

Table 2-5 PMU Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
AVDD1P Output Voltage	10 µF at output pin, connected to AVDD1**	0.950	1.0	1.050	V
DVDD1P Output Voltage	10 µF at output pin, connected to DVDD1**	0.750	1.1	1.150	V
VDDIOP Output Voltage	10 µF at output pin, connected to VDDIO** and VDDPA**	1.65	1.8	1.94	V
VAUX Output Voltage	10 µF at output pin	3.0	3.2	3.5	V

* Values in this table do not include the effects of switching regulator ripple, and are measured using an SDK app in either idle mode or hibernate mode.

** Conditions include any additional bypass cap or filter on the load end (AVDD1, DVDD1, etc).

Table 2-6 GPIO Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Input VIH		VDDIO * 0.7			V
Input VIL				VDDIO * 0.3	V

[1] >= 90% wakeup success rate

Parameter	Conditions	Min	Typ	Max	Unit
Output VOH	2 mA Load, PDSN=0				
	VDDIO = 3.3 V		3.27		V
	VDDIO = 1.8 V		1.76		V
	2 mA Load, PDSN=1				
	VDDIO = 3.3 V		3.25		V
	VDDIO = 1.8 V		1.71		V
Output VOL	2 mA Load, PDSN=0				
	VDDIO = 3.3 V		0.02		V
	VDDIO = 1.8 V		0.03		V
	2 mA Load, PDSN=1				
	VDDIO = 3.3 V		0.04		V
	VDDIO = 1.8 V		0.06		V
Drive Strength, push-pull high	VPIN=VDDIO-0.3V				
	VDDIO = 3.3 V, PDSN=0		21		mA
	VDDIO = 3.3 V, PDSN=1		11		mA
	VDDIO = 1.8 V, PDSN=0		12		mA
	VDDIO = 1.8 V, PDSN=1		6		mA
Drive Strength, push-pull low	VPIN is 0.3V				
	VDDIO = 3.3 V, PDSN=0		27		mA
	VDDIO = 3.3 V, PDSN=1		14		mA
	VDDIO = 1.8 V, PDSN=0		17		mA
	VDDIO = 1.8 V, PDSN=1		8		mA
Pull-up/down Resistance			125		kΩ

Table 2-7 Application ADC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Resolution			11		bits
Effective Number of Bits			9		bits
Sampling Rate	Raw, one channel SDK driver		2 1		MS/s ms
Input Signal Range	VDDIO = 3.3 V VDDIO < 3.3 V	0 0		3.2 VDDIO	V
Reference Voltage			1		V
SNDR			55		dB
INL[1]			3		LSB
DNL[1]			3		LSB
Input capacitance	External Channels, 2 MHz input signal[2]		400		fF
Channel Switching Time			31		µs
Conversion Time	Using SDK driver		900		µs
Measurement Accuracy	Temperature Voltage (Single Channel) Voltage (Differential Channel) Li-ion Battery		±17 ±10 ±20 ±20		°C mV mV mV

[1] Measurement with gain_sel=0, external single channel

[2] External channels on P4-P7 may have extra capacitance due to PCB design.

Table 2-8 Radio Power Consumption

Radio Power Consumption **VBAT current at 3 V with internally or externally generated I/O supply**					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Radio Receiver Rx	Sensitivity at -95 dBm All Rates, max gain, search, or data reception.		0.85		mA
Radio Transmitter Tx	Output power at 0 dBm		2.5		mA

Table 2-9 SoC Power Consumption (3 V)

SoC Power Consumption **VBAT current at 3 V with internally generated I/O supply** (Active RX and Active Tx SoC Power Consumption includes Radio Power Consumption)					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Active RX	All Rates, max gain search, or data demodulation		1.4		mA
Active TX	Output power at				
	10 dBm		12.9		mA
	8 dBm		9.3		mA
	6 dBm		8.2		mA
	4 dBm		4.2		mA
	2 dBm		3.4		mA
	0 dBm		3.0		mA
	-2 dBm		2.7		mA
	-4 dBm		2.4		mA
	-6 dBm		2.1		mA
	-8 dBm		1.8		mA
	-10 dBm		1.6		mA
	-20 dBm		1.2		mA
MCU Active (16 MHz)	Executing CoreMark from RAM at 16 MHz		0.9		mA
MCU Active (64 MHz)	Executing CoreMark from RAM at 64 MHz		2.8		mA
MCU Idle + Bluetooth LE Deep Sleep			0.5		mA
Retention	0 KB RAM (None)		1.8		µA
	32 KB RAM		1.8		µA
	128 KB RAM (Full)		2.1		µA
Hibernation	Timer based wakeup		1.3		µA

SoC Power Consumption VBAT current at 3 V with internally generated I/O supply (Active RX and Active Tx SoC Power Consumption includes Radio Power Consumption)					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Hibernation with Harvesting Enabled	Timer based wakeup		1.6		µA
Hibernation with Wakeup Receiver			1.6		µA
SoC Off	Timer based wakeup		400		nA
Powerdown	PWD pin asserted		120		nA

Note: For a detailed description of low power consumption modes, refer to “Understanding Low Power Modes for ATM33/e Series”

Table 2-10 SoC Power Consumption (4.2 V)

SoC Power Consumption VBATLI current at 4.2 V with internally generated I/O supply (Active RX and Active Tx SoC Power Consumption includes Radio Power Consumption)					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Active RX	All Rates, max gain search, or data demodulation		1.4		mA
Active TX	Output power at				
	10 dBm		13		mA
	8 dBm		9.3		mA
	6 dBm		8.0		mA
	4 dBm		4.0		mA
	2 dBm		3.4		mA
	0 dBm		3.0		mA
	-2 dBm		2.7		mA
	-4 dBm		2.4		mA
	-6 dBm		2.1		mA
	-8 dBm		1.8		mA

	-10 dBm -20 dBm		1.6 1.2		mA mA
MCU Active (16 MHz)	Executing CoreMark from RAM at 16 MHz		0.9		mA
MCU Active (64 MHz)	Executing CoreMark from RAM at 64 MHz		2.9		mA
MCU Idle + Bluetooth LE Deep Sleep			0.5		mA
Retention	0 KB RAM (None) 32 KB RAM 128 KB RAM (Full)		2.1 2.1 2.4		µA µA µA
Hibernation	Timer based wakeup		1.6		µA
Hibernation with Wakeup Receiver			1.9		µA
SoC Off	Timer based wakeup		900		nA
Powerdown	PWD pin asserted		400		nA

Note: For a detailed description of low power consumption modes, refer to “Understanding Low Power Modes for ATM33/e Series”

Table 2-11 Energy Harvesting

Symbol	Parameter	Min	Typ	Max	Unit
VHARV	Cold Start Voltage		0.5		V
	Steady State Regulated Voltage	0.4		3.3	V
	Input Current @ 3 V	1		10,000	µA
VSTORE	Voltage			3.3	V
HARV_IN	RF Input Level (operation) @ 915 MHz	-18		10	dBm
	RF Input Level (operation) @ 2450 MHz	-15		10	dBm
	Frequency Range	400		2500	MHz

Table 2-12 NVM/RRAM Characteristics

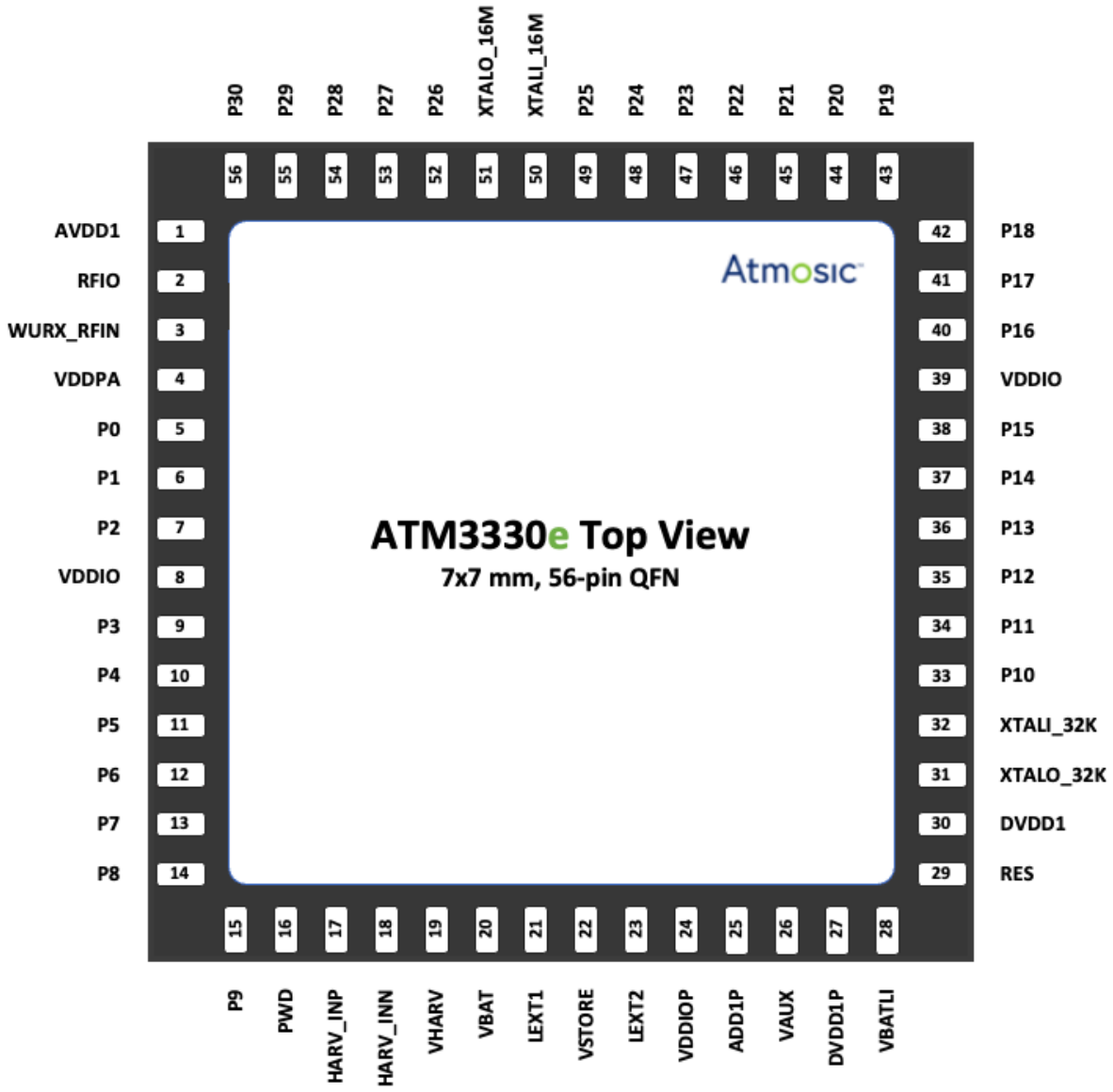
Symbol	Parameter	Min	Typ	Max	Unit
VDDIO		1.62	1.8	3.6	V
Write Endurance		10K			Cycles
Data Retention		10			Years
Read Cycle (4-bytes)	Current (@1.8V) Duration		0.35 0.400		mA µs
Write Cycle (4-bytes) Pattern: 0xaa->0x55	Current (@1.8V) Duration		4.6 180		mA µs

3 Pinout Description

3.1 ATM3330E-5DCAQN 7x7 mm, 56-pin QFN Pinout

The ATM3330e 7x7 mm version is packaged in a Quad Flat Package No Leads (QFN). The pin assignment is shown Table 3.1-1. All pins are on the bottom side of the package.

Figure 3.1-1 ATM3330E-5DCAQN 7x7 mm, 56-Pin QFN Pinout (Top View)



Pin Type Definitions	
Pin Type	**Definition**
I/O	Signal Input or Output
RF	Radio Frequency
PWR	Power supply
A	Analog
R	Reserved
NC	No connection, must be open
GND	Ground

NOTE: Highlighted in gray are signals not supported by the ATM3330e 5x5mm QFN package (P2, P3, P6, P7, P8, P9, P10, P11, P12, P13, P14, P23, P24, P26, P28).

Table 3.1-1 ATM3330E-5DCAQN 7x7 mm, 56-pin QFN Pin Description

7x7 mm, 56-pin QFN Pin Description			
Pin Number	**Name**	**Type**	**Description**
1	AVDD1	PWR	Analog and RF core power supply
2	RFIO	RF	2.4 GHz Single-ended RF I/O for Bluetooth radio
3	WURX_RFIN	RF	Wakeup receiver RF input
4	VDDPA	I/O	PA power supply
5	P0	I/O	Programmable Digital I/O
6	P1	I/O	Programmable Digital I/O
7	P2	I/O	Programmable Digital I/O
8	VDDIO	PWR	Digital I/O Power Supply
9	P3	I/O	Programmable Digital I/O or Analog Input
10	P4	I/O	Programmable Digital I/O or Analog Input
11	P5	I/O	Programmable Digital I/O or Analog Input
12	P6	I/O	Programmable Digital I/O or Analog Input
13	P7	I/O	Programmable Digital I/O or Analog Input
14	P8	I/O	Programmable Digital I/O
15	P9	I/O	Programmable Digital I/O

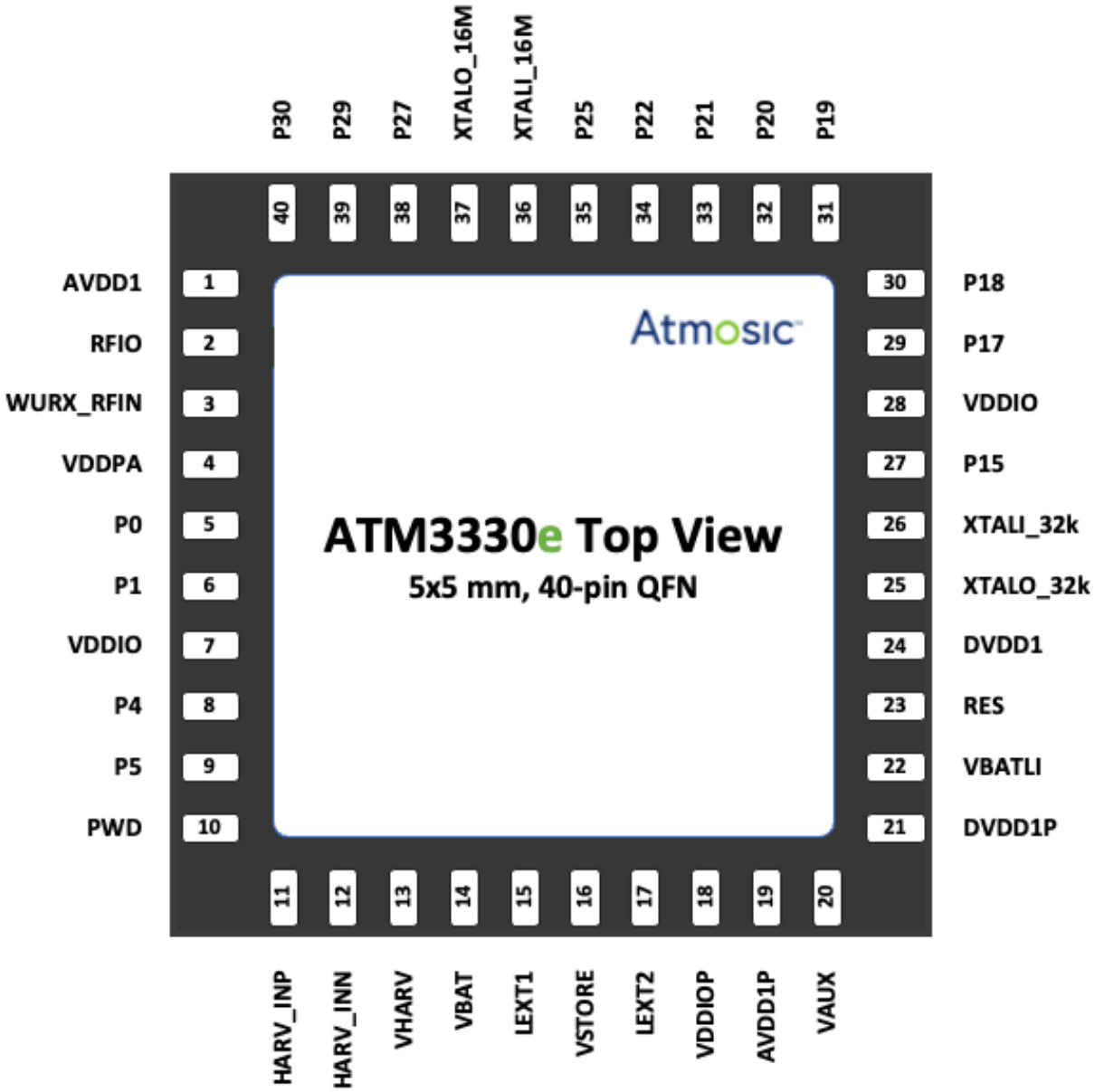
16	PWD	I/O	Power Down Input (Active High)
17	HARV_INP	RF	Differential RF Harvester Input (positive), should be grounded when the RF Harvester is not used.
18	HARV_INN	RF	Differential RF Harvester Input (negative), should be grounded when the RF Harvester is not used
19	VHARV	A	Output of RF Harvester can be used as input from other harvesting modalities to supply energy to the ATM chip, should be grounded when the harvester is not used
20	VBAT	PWR	Battery supply. Must connect to 10 µF capacitor if VBATLI is used.
21	LEXT1	A	Switcher Inductor
22	VSTORE	PWR	Storage node for Switching regulator
23	LEXT2	A	Switcher Inductor
24	VDDIOP	PWR	1.8 V I/O power supply generated by switcher
25	AVDD1P	PWR	1 V Analog and RF core power supply generated by switcher
26	VAUX	PWR	Reserved for switching regulator internal use
27	DVDD1P	PWR	1 V Digital core power supply generated by switcher
28	VBATLI	PWR	2.7 V to 4.2 V lithium ion battery supply in place of VBAT. If lithium ion battery is not used, this pin is recommended to be connected to VBAT.
29	RES	R	Reserved, must tie to ground.
30	DVDD1	PWR	1 V Digital core power supply
31	XTALO_32k	A	32.768 kHz crystal oscillator output
32	XTALI_32k	A	32.768 kHz crystal oscillator input
33	P10	I/O	Programmable Digital I/O
34	P11	I/O	Programmable Digital I/O
35	P12	I/O	Programmable Digital I/O
36	P13	I/O	Programmable Digital I/O
37	P14	I/O	Programmable Digital I/O
38	P15	I/O	Programmable Digital I/O
39	VDDIO	PWR	Digital I/O Power Supply

40	P16	I/O	Programmable Digital I/O
41	P17	I/O	Programmable Digital I/O
42	P18	I/O	Programmable Digital I/O
43	P19	I/O	Programmable Digital I/O
44	P20	I/O	Programmable Digital I/O
45	P21	I/O	Programmable Digital I/O
46	P22	I/O	Programmable Digital I/O
47	P23	I/O	Programmable Digital I/O
48	P24	I/O	Programmable Digital I/O
49	P25	I/O	Programmable Digital I/O, a weak pull low is required during MPU boot.
50	XTALI_16M	A	16 MHz crystal oscillator input
51	XTALO_16M	A	16 MHz crystal oscillator output
52	P26	I/O	Programmable Digital I/O
53	P27	I/O	Programmable Digital I/O
54	P28	I/O	Programmable Digital I/O
55	P29	I/O	Programmable Digital I/O
56	P30	I/O	Programmable Digital I/O
EPAD	VSS	GND	Ground supply for all circuits. The 56-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS.

3.2 ATM3330E-5DCAQK 5x5 mm, 40-pin QFN Pinout (under production planning)

The ATM3330e 5x5 mm version is packaged in a 40-pin Quad Flat Package No Leads (QFN). The pin assignment is shown in Table 3.2-1 . All pins are on the bottom side of the package.

Figure 3.2-1 ATM3330E-5DCAQK 5x5 mm, 40-Pin QFN Pinout (Top View)



Pin Type Definitions	
Pin Type	**Definition**
I/O	Signal Input Output
RF	Radio Frequency
PWR	Power supply
A	Analog
R	Reserved
NC	No connection, must be open
GND	Ground

Table 3.2-1 ATM3330E-5DCAQK 5x5 mm, 40-pin QFN Pin Description

5x5 mm, 40-pin QFN Pin Description			
Pin Number	**Name**	**Type**	**Description**
1	AVDD1	PWR	Analog and RF core power supply
2	RFIO	RF	2.4 GHz Single-ended RF I/O for Bluetooth radio
3	WURX_RFIN	RF	Wakeup receiver RF input
4	VDDPA	PWR	PA power supply
5	P0	I/O	Programmable Digital I/O
6	P1	I/O	Programmable Digital I/O
7	VDDIO	PWR	Digital I/O Power Supply
8	P4	I/O	Programmable Digital I/O or Analog Input
9	P5	I/O	Programmable Digital I/O or Analog Input
10	PWD	I/O	Power Down Input (Active High)
11	HARV_INP	RF	Differential RF Harvester Input (positive), should be grounded when the RF Harvester is not used
12	HARV_INN	RF	Differential RF Harvester Input (negative), should be grounded when the RF Harvester is not used
13	VHARV	A	Output of RF Harvester can be used as input from other harvesting modalities to supply energy to the ATM chip, should be grounded when the harvester is not used
14	VBAT	PWR	Battery supply. Must connect to 10 µF capacitor if VBATLI is used.
15	LEXT1	A	Switcher Inductor

16	VSTORE	PWR	Storage node for switching regulator
17	LEXT2	A	Switcher Inductor
18	VDDIOP	PWR	1.8 V I/O power supply generated by switcher
19	AVDD1P	PWR	1 V Analog and RF core power supply generated by switcher
20	VAUX	PWR	Reserved for switching regulator internal use
21	DVDD1P	PWR	1 V Digital core power supply generated by switcher
22	VBATLI	PWR	2.7 V to 4.2 V lithium ion battery supply in place of VBAT. If lithium ion battery is not used, this pin is recommended to be connected to VBAT.
23	RES	R	Reserved, must tie to ground.
24	DVDD1	PWR	1 V Digital core power supply
25	XTALO_32k	A	32.768 kHz crystal oscillator output
26	XTALI_32k	A	32.768 kHz crystal oscillator input
27	P15	I/O	Programmable Digital I/O
28	VDDIO	PWR	Digital I/O Power Supply
29	P17	I/O	Programmable Digital I/O
30	P18	I/O	Programmable Digital I/O
31	P19	I/O	Test Mode Control
32	P20	I/O	Programmable Digital I/O
33	P21	I/O	Programmable Digital I/O
34	P22	I/O	Programmable Digital I/O
35	P25	I/O	Programmable Digital I/O, a weak pull low is required during MPU boot.
36	XTALI_16M	A	16 MHz crystal oscillator input
37	XTALO_16M	A	16 MHz crystal oscillator output
38	P27	I/O	Programmable Digital I/O
39	P29	I/O	Programmable Digital I/O
40	P30	I/O	Programmable Digital I/O
EPAD	VSS	GND	Ground supply for all circuits. The 40-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS.

4 Mechanical Drawing

4.1 ATM3330E-5DCAQN 7x7 mm, 56-Pin QFN Package

Figure 4.1-1 ATM3330E-5DCAQN 7x7 mm, 56-Pin QFN Mechanical Drawing

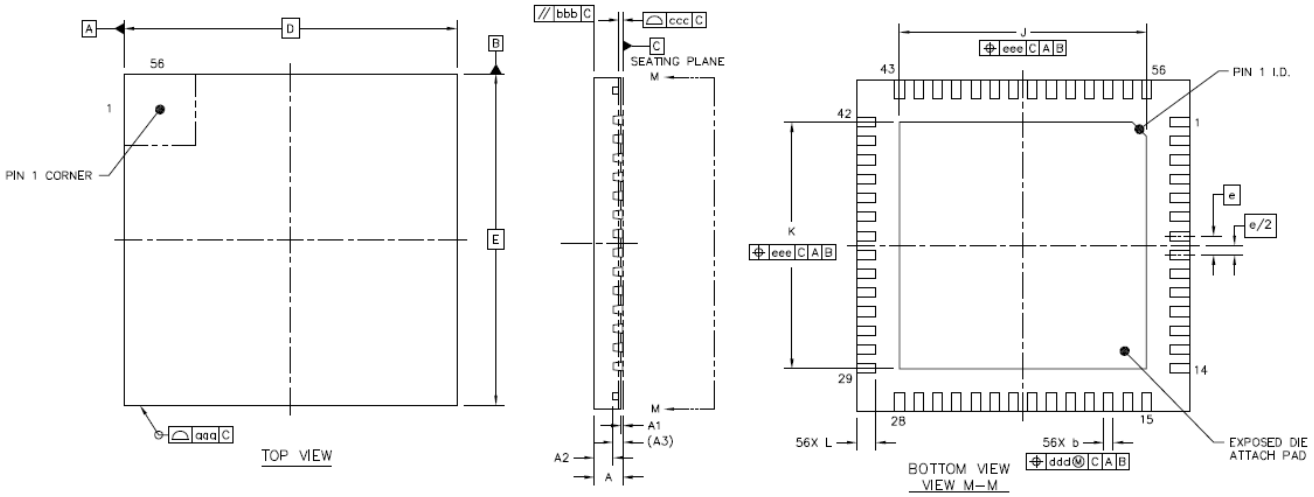


Table 4.1-1 ATM3330E-5DCAQN 7x7 mm, 56-Pin QFN Dimensions

		Symbol	Min	Nom	Max
Total Thickness		A	0.55	0.60	0.65
Stand Off		A1	0	---	0.05
Mold Thickness		A2	0.35	0.40	0.45
L/F Thickness		A3		0.203 REF	
Lead Width		b	0.15	0.2	0.25
Body Size	X	D		7 BSC	
	Y	E		7 BSC	
Lead Pitch		e		0.4 BSC	
EP Size	X	J	5.1	5.2	5.3
	Y	K	5.1	5.2	5.3
Lead Length		L	0.35	0.4	0.45
Package Edge Tolerance		aaa		0.1	
Mold Flatness		bbb		0.1	
Coplanarity		ccc		0.08	
Lead Offset		ddd		0.1	
Exposed Pad Offset		eee		0.1	

Notes:

1. All dimensions are in millimeters.
2. Coplanarity applies to leads, corner leads and die attached pad.

Figure 4.1-2 ATM3330E-5DCAQN 7x7 mm, 56-Pin QFN Land Pattern

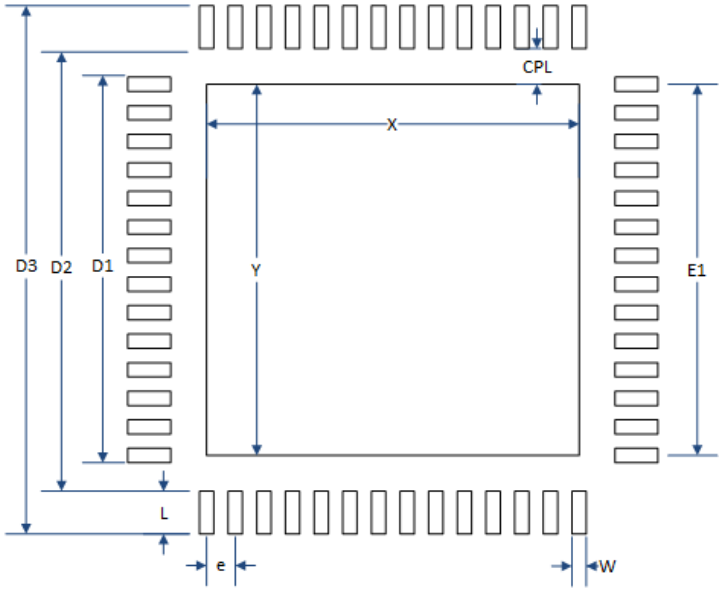


Table 4.1-2 ATM3330E-5DCAQN 7x7 mm, 56-Pin QFN Land Pattern Dimensions

Symbol	Typ
CPL	0.50
D1	5.4
D2	6.2
D3	7.4
e	0.4
E1	5.2
L	0.6
W	0.2
X	5.2
Y	5.2

Notes:

1. All dimensions are in millimeters (mm) unless otherwise noted.
2. The land pattern is based on the IPC-7351 guidelines. There may be other options specified in that publication.
3. The notes above and land pattern are recommendations only. Customers may need to use different parameters as required for their application, materials, SMT process, and tooling requirements.

4.2 ATM3330E-5DCAQK 5x5 mm, 40-pin QFN Package (under production planning)

Figure 4.2-1 ATM3330E-5DCAQK 5x5 mm, 40-Pin QFN Mechanical Drawing

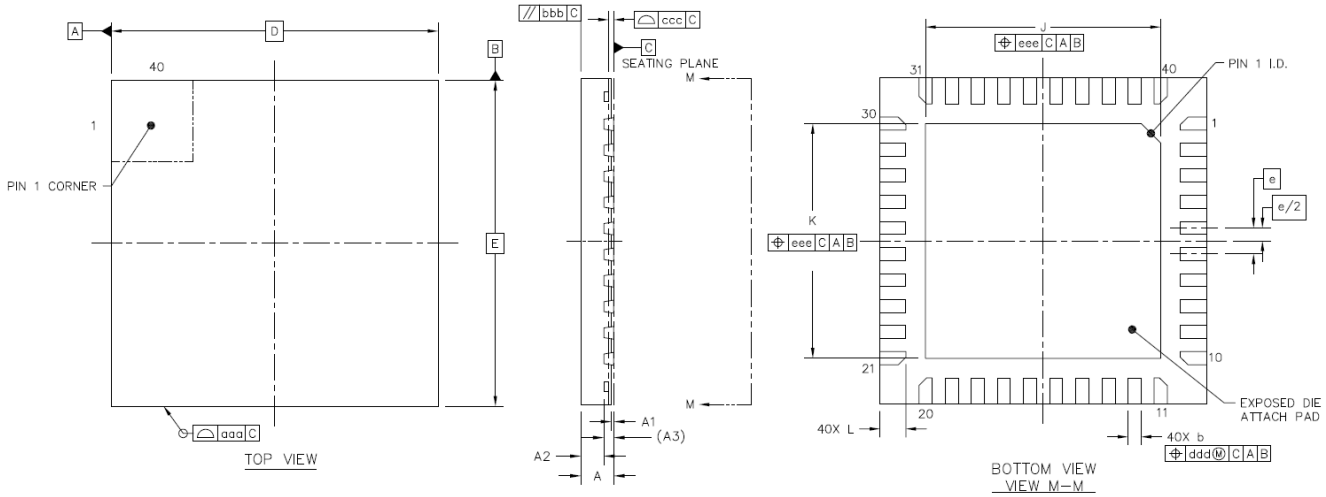


Table 4.2-1 ATM3330E-5DCAQK 5x5 mm, 40-Pin QFN Dimensions

		Symbol	Min	Nom	Max
Total Thickness		A	0.5	0.55	0.6
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	---	0.4	---
L/F Thickness		A3		0.152 REF	
Lead Width		b	0.15	0.2	0.25
Body Size	X	D		5 BSC	
	Y	E		5 BSC	
Lead Pitch		e		0.4 BSC	
EP Size	X	J	3.5	3.6	3.7
	Y	K	3.5	3.6	3.7
Lead Length		L	0.35	0.4	0.45
Package Edge Tolerance		aaa		0.1	
Mold Flatness		bbb		0.1	
Coplanarity		ccc		0.08	
Lead Offset		ddd		0.1	
Exposed Pad Offset		eee		0.1	

Notes:

1. All dimensions are in millimeters.
2. Coplanarity applies to leads, corner leads and die attached pad.

Figure 4.2-2 ATM3330E-5DCAQK 5x5 mm, 40-Pin QFN Landing Pattern

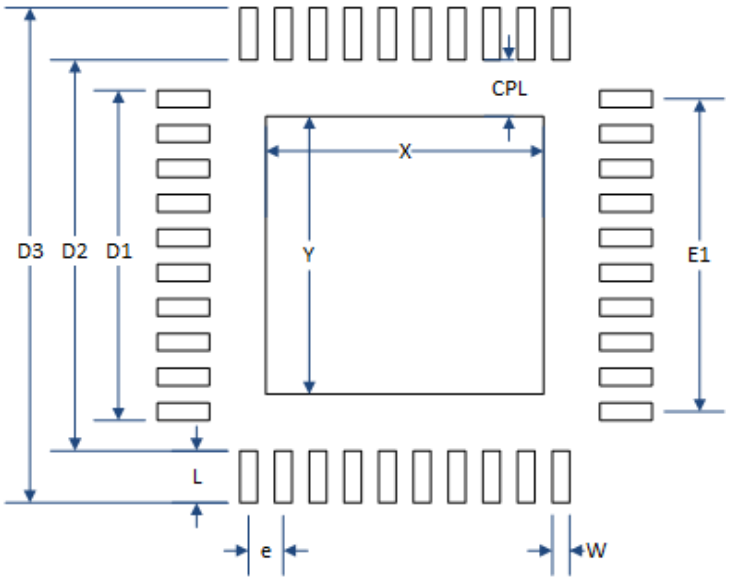


Table 4.2-2 ATM3330E-5DCAQK 5x5 mm, 40-Pin QFN Land Pattern Dimensions

Symbol	Typ
CPL	0.65
D1	3.8
D2	4.5
D3	5.7
e	0.4
E1	3.6
L	0.6
W	0.2
X	3.2
Y	3.2

Notes:

1. All dimensions are in millimeters (mm) unless otherwise noted.
2. The land pattern is based on the IPC-7351 guidelines. There may be other options specified in that publication.
3. The notes above and land pattern are recommendations only. Customers may need to use different parameters as required for their application, materials, SMT process, and tooling requirements.

4.3 Solder Reflow Profile

The recommended reflow profile is per the IPC/JEDEC J-STD-020 specification, for all the packages listed in Mechanical Drawing. Please obtain the official specifications from JEDEC (https://www.jedec.org/).

5 Part Ordering

Table 5-1 Part Ordering Numbers

Part Number	Product Line	Description
ATM3330E-5DCAQN-TR	ATM33 Bluetooth LE Wireless MCU	7x7 mm QFN 56 pin, energy-harvesting, standard Reel, 13” 2.5K devices/reel
ATM3330E-5DCAQN	ATM33 Bluetooth LE Wireless MCU	7x7 mm QFN 56 pin, energy-harvesting, sampling quantity in tray, not for production volume
ATM3330E-5DCAQK-SR (under production planning)	ATM33 Bluetooth LE Wireless MCU	5x5 mm QFN 40 pin, energy-harvesting, small Reel, 7” 1K devices/reel
ATM3330E-5DCAQK (under production planning)	ATM33 Bluetooth LE Wireless MCU	5x5 mm QFN 40 pin, energy-harvesting, sampling quantity in tray, not for production volume

Reference Documents

Document Title	Description	Link
Arm® TrustZone Technology for the Armv8-M Architecture v2.1	TrustZone Architecture Manual	https://developer.arm.com/documentation
Arm® Cortex®-M33 Devices Generic User Guide Revision r1p0	Cortex M33 Users Guide	https://developer.arm.com/documentation
ARM®v8-M Architecture Reference Manual ARM DDI 0553A.e	ARMv8-M Core architecture reference	https://developer.arm.com/documentation
Document Title	**Document Number**	**Link**
ATM33_e Series Reference Manual	ATM33_e-RM	Please submit a request to the Atmosic support portal for access credential.

Revision History

Date	Version	Description
February 13, 2026	0.89	Updated SoC Power Consumption (3 V) and SoC Power Consumption (4.2 V) - Added "Timer based wakeup" condition for Hibernation and SoC Off; Updated Pinout Description - remove "connect to VAUX if unused" for VDDIOP
October 27, 2025	0.88	Updated Functional Block Diagram (remove R-Cache); Updated PMU Characteristics (Conditions for VDDIOP and VAUX)
December 26, 2024	0.87	Update Table 2-9, remove SoC with Energy Harvesting
November 12, 2024	0.86	Update Table 4.1-2 - D1, D3
October 29, 2024	0.85	Update 1.9 Peripherals and I/O - update PWM upper frequency range from 10MHz to 8MHz
September 19, 2024	0.84	Updated Figure 3.1-1, Figure 3.2-1 (remove pin-1 bottom notch marking from package top-view)
September 11, 2024	0.83	Updated Table 2-1
June 19, 2024	0.82	Added Table 2-10 SoC Power Consumption
December 6, 2023	0.81	Updated Table 2-2 Recommended Operating Conditions
November 2, 2023	0.80	Updated Table 2-1 Maximum Electrical Ratings
August 30, 2023	0.79	Updated Table 2-2 Recommended Operating Conditions.
August 23, 2023	0.78	Format change, no content change.
July 28, 2023	0.77	Updated Clocks section, bullet PDM and I2S, MHz to kHz. Table 2-1 Maximum Electrical Ratings, Table 2-2 Recommended Operating Conditions, Table 2-3 Radio Transceiver Characteristics, Table 2-5 PMU Characteristics, Table 2-6 GPIO Characteristics, Table 2-8 Radio Power Consumption,
June 12, 2023	0.76	Added Figure 4.1-2 7x7 mm, 56-Pin QFN Land Pattern, Table 4.1-2 7x7 mm, 54-Pin QFN Land Pattern Dimensions, Figure 4.2-2 5x5 mm, 40-Pin QFN Land Pattern, Table 4.2-1 5x5 mm, 40-Pin QFN Land Pattern Dimensions. Updated Table 2-2 Recommended Operating Conditions, Table 2-5 PMU Characteristics, Table 2-6 GPIO Characteristics.

Date	Version	Description
May 26, 2023	0.75	Updated Overview, Features, Peripherals and I/O, I2C bullet, Table 2-1 Maximum Electrical Ratings, Table 2-2 Recommended Operating Conditions, Table 2-5 PMU Characteristics, Table 2-6 GPIO Characteristics, Table 2-9 SoC Power Consumption.
April 3, 2023	0.74	Updated Table 2-7 Application ADC Characteristics.
April 3, 2023	0.73	Updated Features, Modem, Wakeup Receiver, Configurations, OTP Access sections, Table 2-1 Maximum Electrical Ratings, Table 2-2 Recommended Operating Conditions, Table 2-3 Radio Transceiver Characteristics, Table 2-6 GPIO Characteristics, Table 2-7 Application ADC Characteristics Table 2-8 Radio Power Consumption, Table 2-9 SoC Power Consumption, Table 3.1-1 7x7 mm, 56-Pin QFN Pin Description, Table 3.2-1 5x5 mm, 40-pin QFN Pin Description, Table 4.1-1 7x7 mm, 56-Pin QFN Dimensions,
January 13, 2023	0.72	Updated PMU Configurations, Peripherals and I/O, Table 1.1-1 System Memory Map, Table 2-1 Maximum Electrical Ratings, Table 2-2 Recommended Operating Conditions, Table 2-9 SoC Power Consumption, Table 3.1-1 7x7 mm, 56-pin QFN Pin Description, Table 3.2-1 5x5 mm, 40-pin QFN Pin Description
December 6, 2022	0.71	Updated Features, IR mode under Peripherals and I/O, Table 2-3 Radio Transceiver Characteristics, Table 2-4 Wakeup Receiver Characteristics
November 15, 2022	0.70	Updated VBATLI description in Table 1.4-1 PMU External Pins, Table 3.1-1 5x5 mm, 40-pin QFN Pin Description and Table 3.2-1 7x7 mm, 56-pin QFN Pin Description; updated Table 2-7 Application ADC Characteristics, Table 2-9 SoC Power Consumption, Table 2-10 Energy Harvesting. Renamed VDD1A to AVDD1, and updated Power Management Unit (PMU), Figure 3.1-1 7x7 mm, 56-Pin QFN Pinout (Top View), Table 3.1-1 7x7 mm, 56-pin QFN Pin Description, Figure 3.2-1 5x5 mm, 40-Pin QFN Pinout (Top View), Table 3.2-1 5x5 mm, 40-pin QFN Pin Description, Part Ordering section. Updated Table 2-2 Recommended Operating Conditions Table 2-4 Wakeup Receiver Characteristics, Table 2-9 SoC Power Consumption, Table 2-10 Energy Harvesting.
September 26, 2022	0.67	Updated Table 2-10 Energy Harvesting
September 20, 2022	0.66	Updated Features section, Table 2-1 Maximum Electrical Ratings, Table 2-3 Radio Transceiver Characteristics, Table 2-7 Application ADC Characteristics, Table 2-9 SoC Power Consumption.

Date	Version	Description
September 14, 2022	0.65	Corrected typos, no content change.
September 6, 2022	0.64	Updated Features, Pin Multiplexing, Table 1.1-1 System Memory Map, Table 2-1 Maximum Electrical Ratings Table 2-2 Recommended Operating Conditions, Table 2-9 SoC Power Consumption,
August 16, 2022	0.63	Updated Table 2-1 Maximum Electrical Ratings, Table 2-2 Recommended Operating Conditions, Table 2-3 Radio Transceiver Characteristics, Table 2-5 PMU Characteristics, Table 2-6 GPIO Characteristics, Table 2-7 Application ADC Characteristics, Table 2-9 SoC Power Consumption, Table 2-11 RRAM Characteristics, Part Ordering section; corrected typos, VBALTLI should be VBATLI.
June 14, 2022	0.62	Updated Quad SPI, FLASH, Table 2-11 RRAM Characteristics.
June 8, 2022	0.61	Updated Table 5-1 Part Ordering Numbers.
June 1, 2022	0.60	Updated Clocks, Backplane clock bullet.
May 13, 2022	0.59	Updated Features, GPIO Characteristics, Application ADC Characteristics, SoC Power Consumption, 7x7 mm, 56-pin QFN Pin Description. Added RRAM Characteristics.
March 4, 2022	0.58	Updated VBATLI pin description, corrected typos.
February 22, 2022	0.57	Updated SoC Power Consumption.
February 15, 2022	0.56	Updated Overview section.
February 15, 2022	0.55	Updated Overview, Part Ordering sections.
January 31, 2022	0.54	Added wakeup receiver information Wakeup Receiver and in Pinout Description, added Wakeup Receiver Characteristics and Radio Power Consumption tables, corrected typos.
December 3, 2021	0.53	Changed part number, updated Overview, Pinout Description, Part Ordering sections, corrected typos.
November 9, 2021	0.52	Updated MCU & Memory, Pinout Description, Part Ordering sections, corrected typos.

Date	Version	Description
October 31, 2021	0.51	Changed format. Updated MCU & Memory , Security, Sensor Hub, Timers and Interrupts, Peripherals and I/O, Electrical Specification sections.
August 20, 2021	0.50	Initial version created.

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