ATM34/e Series Hardware

Design Guide

SUMMARY: This document describes how to implement hardware designs with the ATM34/e Wireless SoC Series, including layout guidelines, RF matching guidelines, digital I/O connections, and PMU (Power Management Unit) configuration.

Atmosic™

ATM34 Series Hardware Design Guide
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Acronyms and Abbreviations

Acronyms	Definition
ATM33/e	ATM3330e ATM3330 ATM3325
ATM34e	ATM3430e
ATM34	ATM3430 ATM3405
ATM34/e	ATM3430e ATM3430 ATM3405
EVB	Evaluation Board
EVK	Evaluation Kit
NVM	Non-Volatile Memory
PMU	Power Management Unit
RAM	Random Access Memory
ROM	Read-Only Memory
SoC	System-on-Chip

1. Overview

The ATM34/e Wireless SoC Series is part of a family of extreme low-power Bluetooth® SoC devices. This SoC offers Bluetooth Low Energy support with an ARM® Cortex® M33F application processor, 256 KB RAM, 64 KB ROM, 512-2560KB NVM, with ARM® TrustZone® enabled security features, and state-of-the-art power management to enable maximum lifetime in battery-operated devices.

This document describes how to implement hardware designs with the devices listed in Table 1. Table 1 also lists the EVKs applicable to this document.

EVK	SoC Package	SoC Part Number	Kit Part Number
Evaluation Kit for ATM3430e 7x7 QFN	56-pin 7x7 mm QFN	ATM3430E-5YCAQN	ATMEVK-3430e-YQN-5
Evaluation Kit for ATM3405 BGA	93-ball 4x4 mm BGA	ATM3405-5YCABV	ATMEVK-3405-YBV-5
Evaluation Kit for ATM3405 5x5 QFN	40-pin 5x5 mm QFN	ATM3405-5WCAQK ATM3405-5PCAQK	ATMEVK-3405-WQK-5

Table 1 - ATM34/e Series EVKs

The following topics are covered:

- Migrating from ATM33/e
- PMU Configurations
- I/O Connections
- Component Selection
- Layout Guidelines
- Matching Guidelines
- Production Test Guidelines

2. Migrating from ATM33/e

When migrating a hardware design from ATM33/e to ATM34/e, please note the following differences that may trigger design changes:

- The ATM33/e and ATM34/e have different RFIO impedances.
- The ATM34/e only has one PDM core, so ATM33/e designs using the PDM1 interface pins will need to be remapped to use PDM0 interface pins.
- The ATM34/e supports I2C clock stretching, so an external pull-up resistor on I2C_SCL may be desired.
- The ATM3430 and ATM3430e include extended NVM, so an external flash should not be needed when migrating from ATM3330 or ATM3330e.

3. PMU Configuration

Please refer to the Supported PMU Configurations section of the **ATM34/e Series Reference Manual** for battery and I/O supply options. The following questions may help determine the correct configuration:

- What is the voltage range of the primary power source?
  - For voltage levels greater than 3.6 V, VBATLI must be used, and VBAT must be connected to a bypass capacitor (10 µF).
  - For voltage levels between 1.1 V and 3.6 V, VBAT should be used and should also be connected to VBATLI.
- Does the I/O supply need to be internally generated (i.e., VDDIO connected to VDDIOP)?
  - If VBAT is between 1.1 V and 1.8 V, the I/O supply must be internally generated.
- Do on-board peripherals require an external I/O supply?
  - If the ATM34/e is interfacing to peripherals (e.g., Flash, sensors, etc), they must share an I/O supply. If a peripheral I/O supply needs to be greater than 1.8 V, an external I/O supply is needed.
  - The ATM34/e is able to power peripherals from its internally generated I/O supply up to an average of 25 mA. If the combined current consumption of all peripherals can exceed this value, an external I/O supply is needed.

    ***Note**: The ATM34/e PMU can sustain a maximum average load of 100 mW (measured at VBAT), which includes the ATM34/e as well as any peripherals that are being powered.*
  - When using VBATLI, the ATM34/e can sustain a maximum of 0.5mA from its internally generated I/O supply during low power states. If the combined current consumption of all peripherals can exceed this value while the ATM34/e is in a low-power state, an external I/O supply is needed.
- What is the maximum transmit output power for the application?
  - If the maximum transmit output power is 4 dBm or lower, it is recommended to connect VDDPA to a bypass capacitor (1 µF).
  - If the maximum transmit output power is greater than 4 dBm, VDDPA must be connected to VDDIOP with a bypass capacitor (1 µF) placed as close as possible to the VDDPA pin.

4. I/O Connections

All of the ATM34/e digital I/O have programmable functionality, and it is recommended to use the Atmosic Pinmux Tool for selecting digital I/O functionality. Each digital I/O also has programmable drive strength and pull options. Please refer to the **ATM34/e Series Datasheet** for details. The following section covers some additional considerations:

- Power Down (PWD) should be pulled low to allow for debug and production test support. Pulses of voltage greater than 0.7 V and greater than 1 ms in duration are required when this pin is used for resetting the chip.
    - For applications where the primary power source can be disconnected or experience large voltage fluctuations for short periods of time, a PWD circuit (such as what is shown in Figure 1) is required to ensure the ATM34/e resets properly.

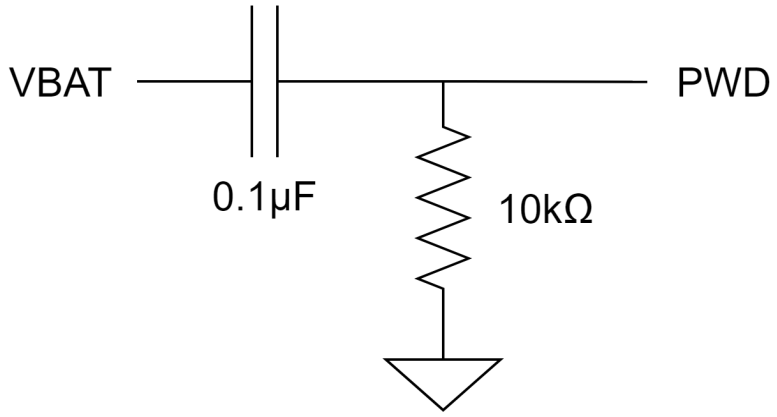

Figure 1 - Circuit to Generate PWD Pulse

The component values may need to be tuned to achieve the required pulse voltage and duration, depending on voltage levels and ramp rate.

- P25 should be pulled low to allow for debug and production test support. P25 must be low during software boot to allow for normal code execution. If P25 is high during software boot, the ATM34/e will enter an idle state suitable for certain operations such as programming or dumping the on-chip NVM. After the software boots, P25 can be reconfigured and used as a normal GPIO. The size of the on-board pull-down resistor should account for any shared functionality. For example, an application that can reset while P25 is outputting high may need a stronger pull-down to ensure the pin is low during software boot after the reset.

- The default state for all ATM34/e digital I/O is high-Z with no internal pull-up or pull-down during Powerdown and SoC Off. In other power states, P0 and P1 default as inputs with an internal pull-down on P0 and an internal pull-up on P1.
- If an onboard resistor divider is connected to an Application ADC input, component values should not exceed 100 kΩ to avoid impacting measurement accuracy. Application ADC inputs should also be routed carefully to minimize noise coupling. Please refer to the **ATM34/e General Purpose ADC Application Note** for voltage ranges and configuration options. If a transistor is being used to enable the resistor divider (such as what is shown in Figure 2), the component values should account for the threshold voltage, and the Application ADC input should be pulled low when the transistor is off.

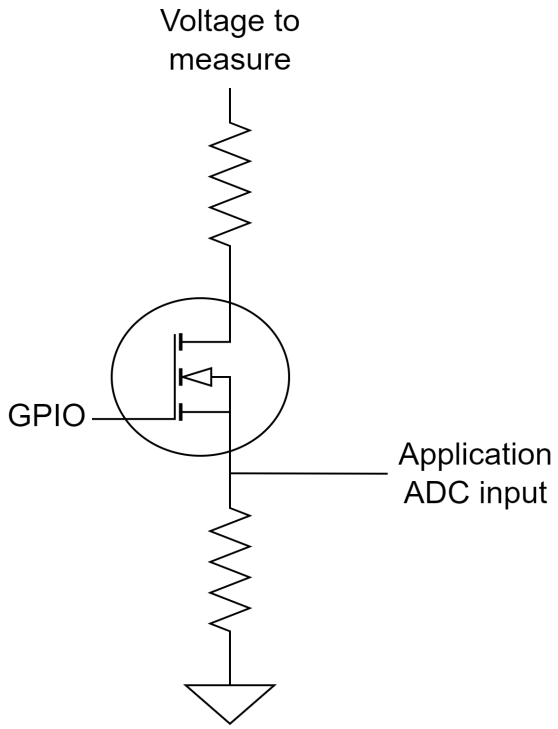

Figure 2 - Voltage Divider with a Transistor for Application ADC

- To support I2C clock stretching, software configures I2C_SCL as open-drain with internal pull-up by default, which may require an on-board pull-resistor depending on the I2C clock frequency.
- For ATM3430 and ATM3430e designs that do not use the Wakeup Radio, the WURX_RFIN pin should be tied to ground.
- For ATM3430e designs that do not use energy harvesting, the VSTORE and VHARV pins should be tied to ground.

- RES, HARV_INP, HARV_INN, and VDDPAP pins should be tied to ground.

5. Component Selection

5.1 Flash

If an external flash is needed, the ATM34/e supports the following QSPI flash families:

Manufacturer	Part Number	ID #
Macronix	MX25Rxx	0x28c2
Gigadevice	GD25WQxx	0x65c8
Winbond	W25QxxEW	0x60ef
Giantec	GT25Qxx	0x40c4
Puya	P25QxxU	0x4085

Table 2 - Serial Flash Families

5.2 16 MHz Crystal

The 16 MHz crystal used on the ATM34/e EVB is the E1SB16E00001KE from Hosonic (+/-10 ppm tolerance, +/-15 ppm stability, 8 pF load capacitance, 80 Ω maximum ESR).

This can be used as a reference when choosing alternate parts (e.g., Epson FA-20H 16.0000MF20X-AJ or ECS ECS-160-8-36-JTN).

The ATM34/e supports up to +/-50 ppm total combined stability and tolerance as required by the Bluetooth 5 specification.

The ATM34/e can support load capacitance up to 12 pF with internal tuning capacitors, but < 9 pF is recommended for lower power consumption.

If an alternate part with a different load capacitance is used, the ATM34/e internal tuning capacitors may need to be adjusted. This can typically be done via lab characterization:

1) Follow the instructions in the **Atmosic RF Test Tool User Guide** (available on the Atmosic Support website) to install and run the Atmosic RF Test Tool.
2) Connect the DUT RF port to a spectrum analyzer.

3) Select the CAL. tab on the Atmosic RF Tool, and click the 16MXtal Cal. button. For each iteration, check the frequency offset on the spectrum analyzer, enter the value (Hz) in the pop-up window, and click Exit. Upon completion, the characterized value between 0 and 31 will be displayed in the Atmosic RF Tool.
4) Repeat step 3 on a handful of DUTs to confirm that the characterized value is similar across multiple devices.
5) Input the characterized value into the Atmosic Production Test Tool to be programmed during DUT manufacturing.

If a TCXO is used, its output needs to be positive (not going below 0V), and the peak-to-peak swing should be as large as possible, up to 2V max. The output should be connected to the XTALI_16M pin, and the XTALO_16M pin should be left floating. The Atmosic Production Test Tool should also be configured to program the device for TCXO operation.

5.3 32.768 kHz Crystal

The 32.768 kHz crystal used on the ATM34/e EVB is the SC20S-7PF20PPM from Seiko Instruments (+/-20 ppm tolerance, 7 pF load capacitance, 70 kΩ maximum ESR).

This can be used as a reference when choosing alternate parts (e.g., Micro Crystal AG CM8V-T1A-32.768KHZ-7PF-100PPM-TA-QC).

The ATM34/e supports up to +/-500 ppm total combined stability and tolerance as required by the Bluetooth 5.3 specification.

The ATM34/e can support load capacitance up to 12 pF with internal tuning capacitors, but < 9 pF is recommended for lower power consumption.

Care must be taken in assembly to avoid excessive solder flux that can create a parasitic impedance path between the two pins XTALI and XTALO. This parasitic PCB impedance must be more than 100Mohms, and the total impedance, combining PCB and the crystal and internal impedance of the chip, must not be less than 12Mohms.

If the application does not require a crystal, the XTALI_32k pin should be grounded, and the XTALO_32k pin should be left floating.

5.4 Switcher Inductor

The 3.3 µH multilayer chip power inductor used by the switcher on the ATM34/e EVB is the LQM2MPN3R3NG0L from Murata. The DC Resistance (DCR) of this inductor is

120/150 mΩ (typical/max), and the rated current is 1.2 A. If choosing an alternate part, it needs to have a similar DCR and a rated current of 600 mA or higher.

5.5 Harvester Storage Capacitor

The ATM34e EVBs by default have 10 µF (C2), 10 uF (C76), and 47 µF (C8) storage ceramic capacitors on VSTORE. More capacitance can be added if more charge storage (up to 484 µF) is desired by installing 220 uF for C8 and C78, and 22 uF for both C2 and C76.

Please note that the effective capacitance of high-density ceramic capacitors typically decreases with increasing applied DC voltage. Please consult the particular capacitor datasheet to arrive at the desired effective capacitance. For example, the Murata 1206 220 µF capacitors have an effective capacitance of approximately 90 µF at 3.0 V. Similarly, the 100 µF capacitors also have a derating of roughly 56 % at 3.0 V, thereby having a capacitance of about 55-60 µF at 3.0 V. Refer to Murata's datasheet.

Besides ceramic capacitors, supercapacitors can also be used as high-capacity storage capacitors. The following supercapacitors have been characterized by Atmosic.

- Korchip SM3R3333 (33 mF)
- Korchip SM3R3703 (70 mF)
- ELNA DSK-3R3H334T (0.33 F)
- ELNA DSK-3R3H204T614 (0.2 F)
- Vinatech WEC 3R0105QG (1F)
- Kamcap HP-3R0-J354VYJ03 (0.35 F)

If a higher internal resistance supercapacitor is selected (ie, Korchip and ELNA supercapacitors from the list above), it is recommended to have a 220 µF ceramic capacitor connected in parallel with the supercapacitor to mitigate the voltage ripple. This filtering ceramic capacitor is necessary for systems with supercapacitors only and no battery.

Please refer to the **ATM33e/ATM34e Support for External Energy Storage Devices Application Note** for more information about energy storage devices for the ATM34e.

5.6 Antenna Switch

If an antenna switch is necessary for Channel Sounding (CS) applications, the ATM34/e EVBs have been characterized with the Murata XMSSJR8G2PA-246 to work well for all channel sounding performance metrics down to T_SW=2 µs (CS antenna switch time). If a different antenna switch is desired, then the following guidelines should be met:

1. The switching time specification is usually defined as a change of amplitude power (say to 10% or 90%) and not how long it takes for an RF carrier tone's phase to settle after switching antenna ports. For a given CS switching time specification (1, 2, 4, or 10 µs), make sure the switching time is sufficiently fast to allow for the phase to settle, such as by measuring the CS phi_zmd specification.
2. 30 dB or higher port isolation.

6. Layout Guidelines

This section describes layout guidelines to be followed on some key signals/routes to/from the ATM34/e.

6.1 RFIO Section

The ATM34/e EVBs have a matching circuit as shown in Figure 3 and component values in Table 3.

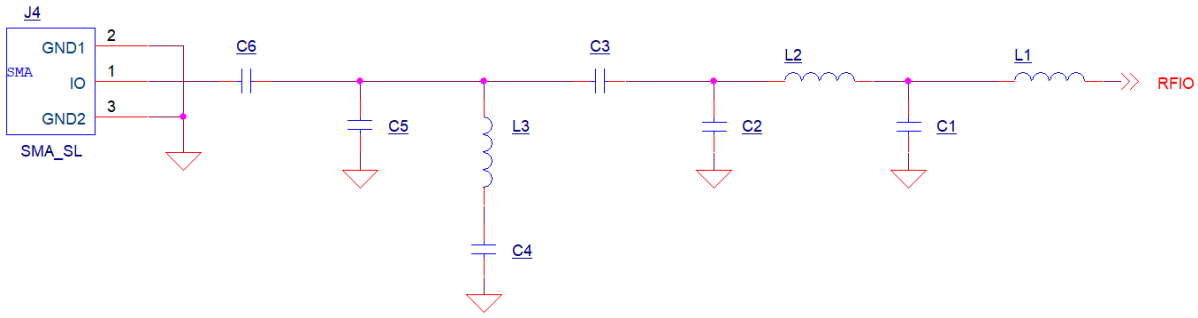

Figure 3 - RFIO Matching Circuit

EVB	Part Reference in Figure 3	Part Reference in EVB	Value
ATM34/e EVB	L1	L11	3.0 nH
	C1	C21	1.5 pF
	L2	L12	2.7 nH
	C2	C20	1.0 pF
	C3	C65	10 pF
	L3	L3	NL
	C4	C22	NL
	C5	C66	NL
	C6	C18	0 Ω

Table 3 - RFIO Matching Circuit

The two series inductors (L1 and L2) and two shunt capacitors (C1 and C2) function as a low-pass filter (assuming a pure 50 Ω termination at all harmonic frequencies) to reject higher harmonic frequencies to meet FCC requirements. To maximize harmonic rejection and minimize fundamental power loss, it is recommended that type MHQ series inductors from TDK or LQP03HQ series inductors from Murata be used. If an antenna with good inherent harmonic rejection is used, this filtering network may be simplified. L1 value may be increased slightly to 3.3nH for the smaller BGA package to compensate for the smaller internal series inductance on the RFIO pin of the package.

The series 10 pF capacitor functions as a DC block and can be placed at C6 or C3, depending on whether the optional notch filter L3/C4 is used, and creates a DC short. C5 is a 0201 footprint placeholder intended for an ESD protection device, which is strongly recommended if the antenna is exposed to external physical contact either during assembly or in the final product and does not provide a low-impedance path to GND. If a PIFA, which has a DC short to GND, is used, an ESD protection device is not needed. Such an antenna is recommended.

An example of such a device is the ESD150-B1-W0201 from Infineon, which can significantly boost the ESD voltage protection beyond the industry standard requirement met by the ATM34/e. This optional extra protection may be used when the board is assembled in an environment where the ESD voltage exceeds that allowed by industry standards. An alternative device with comparable specifications to the ESD150-B1-W0201, especially the clamping voltage and line capacitance, may be used.

As for the placement of these components on the PCB, it is critical that the 4 lowpass filter components (L1, C1, L2, C2) be placed next to each other and as close to the ATM34/e as SMT assembly allows, minimizing any parasitic inductance resulting from the connecting trace, to maximize the effectiveness of the filtering and matching. It is also recommended that C1 and C2 are physically separated and not share a GND via.

Furthermore, the current selection of the values of the filter and matching components listed in Table 3 above assumes the fixed distance between L1 and the ATM34/e on the EVB. In a layout where this distance is different, the values of the filter and matching components will need to be adjusted accordingly. L1 and C1 will be the most likely components to be adjusted to compensate for that distance.

The layout of the EVB PCB has this transmission line modeled as a Coplanar Waveguide (CPW) with a characteristic impedance of 50 Ω. The trace width/spacing can be adjusted according to the board stack-up.

If additional tuning is required, please note that the impedance of the match discussed in Table 3 when looking out from the RFIO port (using a pigtail placed at the RFIO pin,

without the ATM34/e), towards the match is roughly 40+j35 at 2.44 GHz and 6+j80 at 4.88 GHz. This is the load impedance of the ATM34/e PA that will ensure the optimum transmit power, efficiency, and harmonics. This same load will, at the same time, ensure a good match for the receiver.

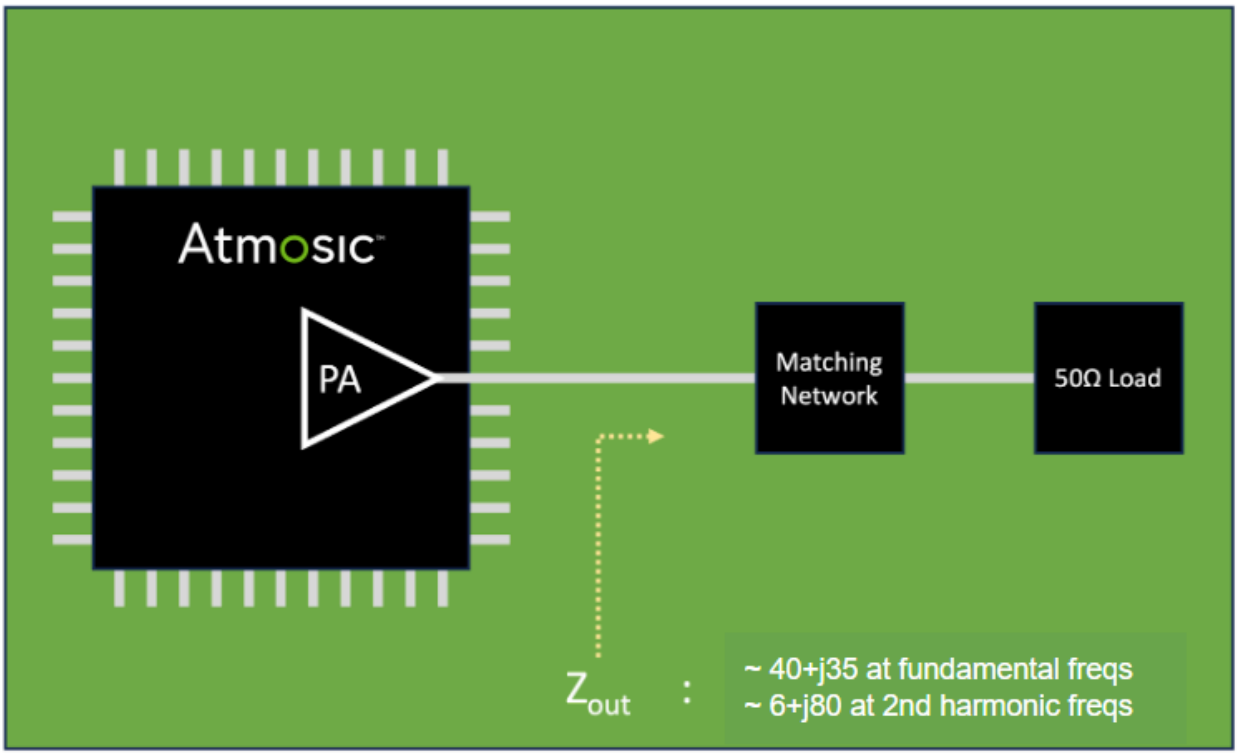

Figure 4 - RFIO Match Circuit Block Diagram

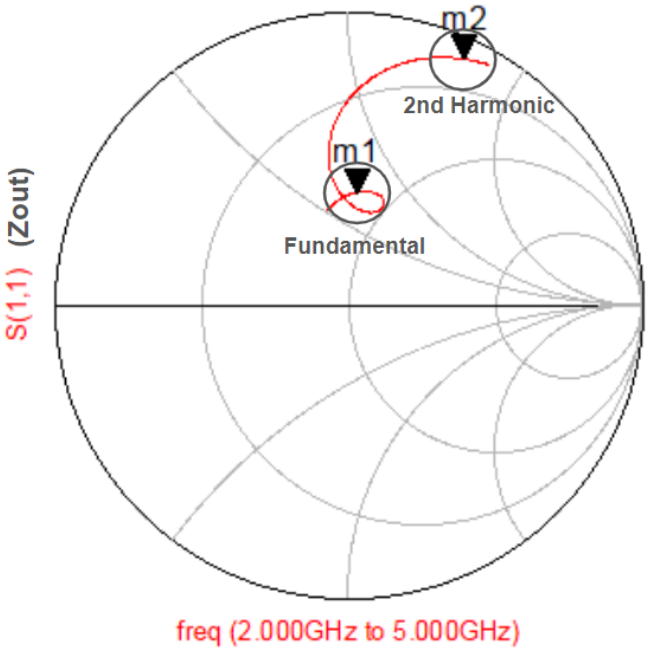

Figure 5 - Simulated RFIO Match S11 Looking Out from the SoC

6.3 Board Stack-up

While the board stack-up can be chosen according to the needs of the application, the stack-up of the current version of ATM34/e EVBs is shown below. The board thickness is 62 mils (or 1.58 mm).

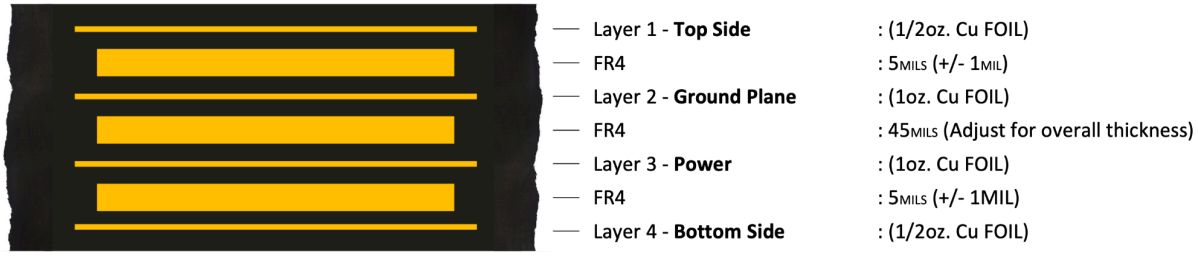

Figure 6 - Board Stack-Up

Also, shown below is an alternative example of a 4-layer stack-up for thinner (32 mils/0.8 mm) PCBs.

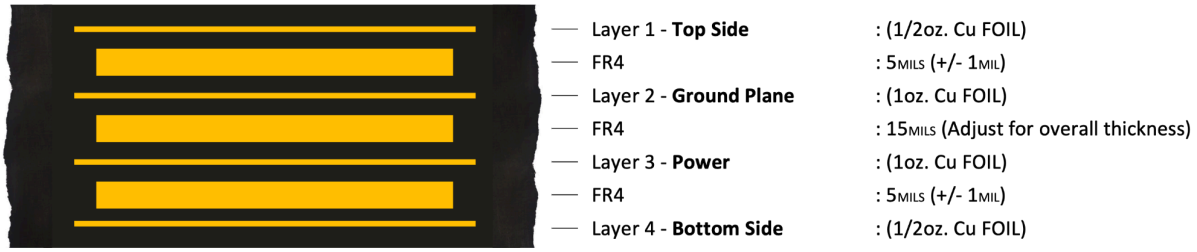

Figure 7 - 4-Layer Stack-up for Thinner PCB

And shown below is the stack-up of the current version of the EVB based on the ATM3405 in a BGA package. The total thickness of this EVB is 61.3 mils. Six layers are needed to allow access to the inner-row pins without perforating the GND plane underneath the chip and using costly via-in-pad technology. This can be accomplished by routing the inner-row pins on Layer 2 through blind vias placed in the free space between the inner row and the center GND pins. Layers 3 and 5 are used as GND planes. Layers 4 and 6 can be used for routing.

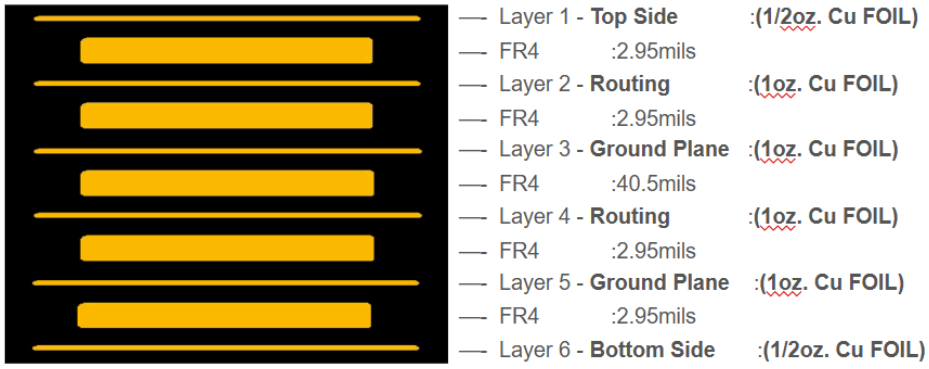

Figure 8 - 6-Layer Stack-up for ATM3405 BGA EVB

6.4 Switcher Inductor

For ATM3430 and ATM3430e-based 4-layer PCBs, the 3.3 µH switcher inductor needs to be placed as close as possible to pins 21 and 23. However, priority is given to the decoupling capacitor connected to pin 20 (VBAT), pin 24 (VDDIOP), and pin 25 (AVDD1P). A trace width of at least 10 mils is recommended to minimize the loop area formed by the traces, inductor, and the Atmosic device. Avoid routing sensitive small analog signals on all layers beneath the inductor. Figure 12 below illustrates a recommended layout for the above-mentioned guideline.

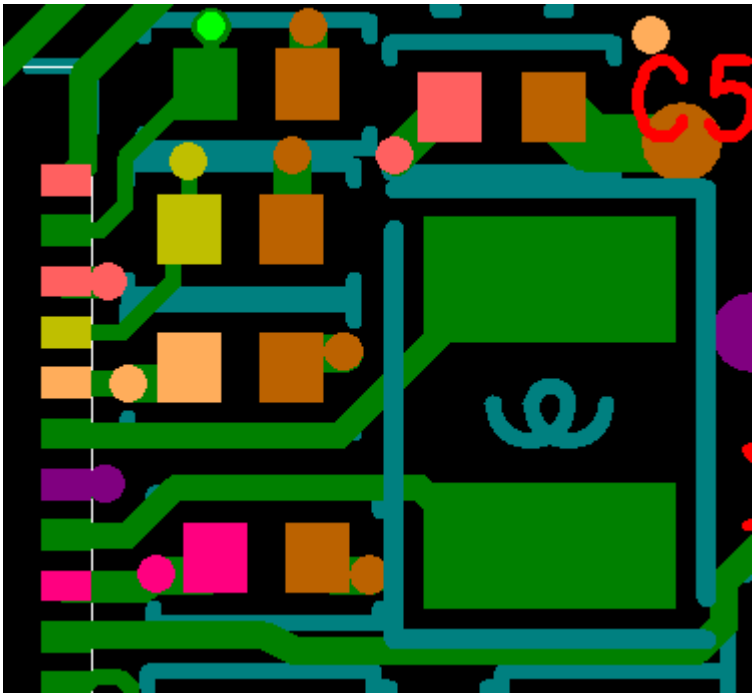

Figure 9 - Switcher Inductor Layout Recommendation for ATM3430 or ATM3430e PCB

For ATM3405 QFN-based 4-layer PCBs, the recommendation is similar to the 7x7 mm package, but its respective pins are different for the inductor and nearby voltage rails: pins 14 and pin 16 for the inductor, and bypass capacitors close to pin 13 (VBAT), pin 17 (VDDIOP), and pin 18 (AVDD1P).

For ATM3405 BGA-based 6-layer PCBs, the recommendation is also similar to the 7x7 mm package, but its respective pins are different for the inductor and nearby voltage rails: pins L6 and L7 for the inductor, and bypass capacitors close to pin L5 (VBAT), pin L8 (VDDIOP), and pin L9 (AVDD1P).

6.5 Connecting AVDD1P to AVDD1

The placement of bypass capacitors on the analog rail and their routing from the AVDD1P pin to the AVDD1 pin is critical to the performance of the PMU and radio blocks:

- Place the 10 µF bypass cap on AVDD1P as close as possible to the pin (pin 18 on ATM34 PCBs with 5x5 mm QFN package, or pin 25 on ATM34/e-based PCBs with 7x7 mm QFN package, or pin L9 on ATM3405 with 4x4 mm BGA package). This capacitor must be placed on the same layer as the ATM34 device.

- While routing AVDD1P to AVDD1 via the RC filter, place the via closer to the AVDD1P bypass capacitor than to the pin/pad itself. In doing so, the AVDD1P pin “sees” less inductance (thus lower impedance) to the bypass capacitor than to the remaining trace.
- Place the RC filter (1 Ω + 20 µF) close to the AVDD1 pin to filter out effectively any noise that may get on the AVDD1P supply trace. The two 10 uF capacitors can be combined into one 22 uF for PCB space saving or cost saving. The AVDD1 supply level should be within +/- 5% for performance and +/- 20% for functionality.

7. Production Test Guidelines

7.1 I/O Connections

The following pins are needed for production test support connections:

- GND
- VBAT or VBATLI for powering the DUT
- PWD for resetting the DUT (pulse is needed after applying power to the DUT)
- P25 for configuring the DUT to the MCU idle state
- P0 for SWDCLK and P1 for SWDIO to program the DUT, or P25 and P27 for optional UART bootloader support
- UART0 for RF testing via DTM (2-wire) or HCI (2-wire or 4-wire) interface

7.2 Programming OTP

The following OTP fields need to be programmed based on the PMU configuration and security requirements:

- otp_disable_xtal32k
- otp_vbatt_level
- otp_batt_type
- rram_write_locks
- uart1_rx_disable
- sec_dbg_config
- rram_jtag_bypass

Please refer to the OTP Memory section of the **ATM34/e Series Reference Manual** for details regarding these fields.

Reference Documents

Title	Document Number
ATM34/e Series Datasheet	6494-xxxx-xxxx
ATM34/e Series Reference Manual	6444-xxxx-xxxx
ATM34/e General Purpose ADC Application Note	6685-xxxx-xxxx
Atmosic RF Test Tool User Guide	ATM-UGRF-0060
ATM33e/ATM34e Support for External Energy Storage Devices Application Note	4266-xxxx-xxxx

Revision History

Date	Version	Description
February 17, 2026	0.15	Updated RFIO Section
January 21, 2026	0.14	Updated PMU Configuration, I/O Connections, 16 MHz Crystal, Switcher Inductor, Antenna Switch, Programming OTP
July 8, 2025	0.13	Updated Migrating from ATM33; PMU Configuration (I/O supply when using VBATLI; VDDPAP connections to VDDIOP); 32.768 kHz Crysta; Antenna Switch; 4x4 BGA package specifics in RFIO Section; Board Stack-up; Connecting AVDD1P to AVDD1 Removed RF Harvester Section
January 7, 2025	0.12	update I/O Connections
July 19, 2024	0.11	adding Migrating from ATM33/e
February 20, 2024	0.10	Initial version created.

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