ATM34/e Series

Extreme Low Power Bluetooth 6.0 SoC with Energy Harvesting

Datasheet

Overview

The ATM34e & ATM34 Series SoCs are members of the Bluetooth Low Energy extreme low-power system-on-chip (SoC) devices from Atmosic. The ATM34/e Series SoCs integrate the Bluetooth 6.0 compliant radios with an ARM® Cortex® M33F application processor, Random Access Memory (RAM), Read-Only Memory (ROM), and nonvolatile memory (NVM), with ARM® TrustZone® enabled security features, and state-of-the-art power management to enable maximum lifetime in battery-operated devices.

The extremely low-power ATM34/e Series SoC comprises several products with resources scaled to encompass the various application and protocol requirements for Bluetooth 6.0 devices. Designed to extend the battery life for the Internet-of-Things, the radio uses only 0.95 mA in receive and only 2.5 mA in transmit at 0 dBm. Support for low-duty cycle operation allows systems to run for significantly extended periods without battery replacement. In addition, this series of SoCs from Atmosic supports operation from energy harvesting sources, including photovoltaic and motion. Innovative wake-up mechanisms are supported to provide options for further power consumption reduction.

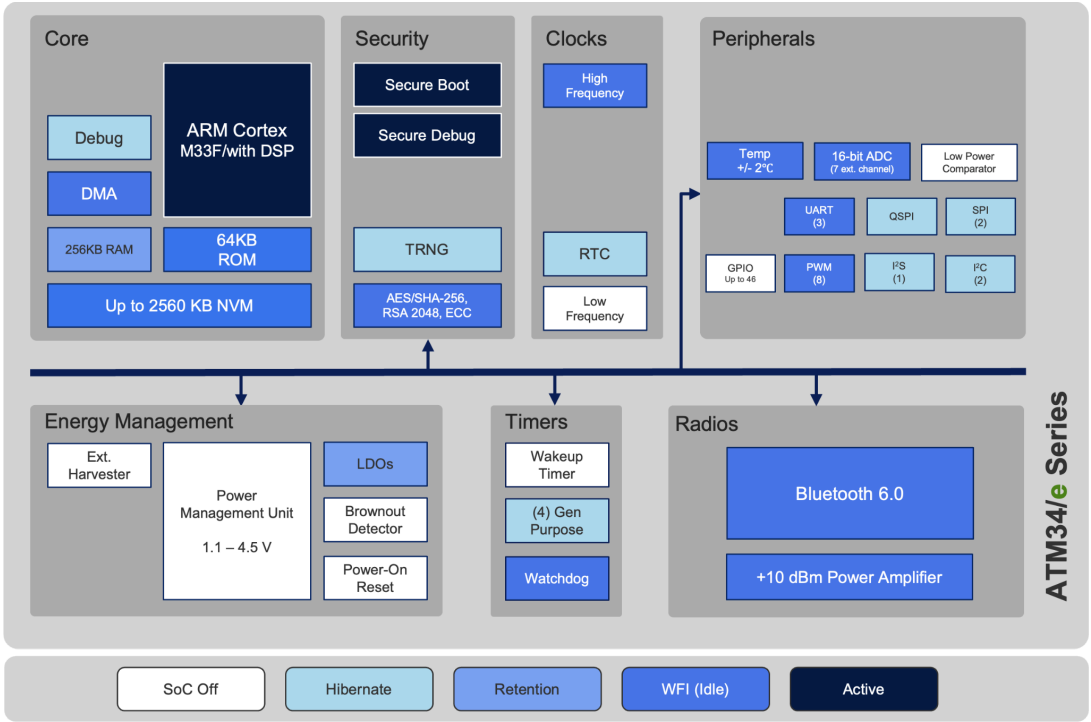
Applications

Industrial and Enterprise

- Asset Tracking
- Industrial IoT Sensors
- Remote Monitors

Home and Consumer

- Asset Tracker and Tags
- Security
- Environmental Control & Advanced Home Automation



Features

Standards Supported

- Bluetooth 6.0
  - Bluetooth Low Energy
  - 2 Mbps, 1 Mbps, & Long Range PHY rates
  - Bluetooth 6.0 Channel Sounding

MCU and Memory

- 64 MHz ARM® Cortex® M33F MCU
- 64 KB ROM, 256 KB RAM, up to 2560 KB NVM
- Retention RAM: 16 KB to 256 KB in 16 KB step sizes
- 16 MHz / Optional 32.768 kHz Crystal Oscillator
- UART bootloader support in ROM

Security

- ARM® TrustZone®, HW Root of Trust, Secure Boot, Secure Execution & Debug
- AES-128/256, SHA-2/HMAC 256 Encryption/Cryptographic Hardware Accelerators
- True random number generator (TRNG)

Energy Harvesting (ATM34e)

- Supports photovoltaic, motion, and other energy harvesting technologies
- External Harvesting/Storage Interface

RF and Power Management

- Fully integrated RF front-end
- 1.1 V to 4.5 V battery input voltage with integrated Power Management Unit (PMU)
- Radio power consumption with a 3 V battery
  - Rx @ -97 dBm: 0.95 mA
  - Tx @ 0 dBm: 2.5 mA
- SoC typ. power use with a 3 V battery with PMU
  - Retention @ 32 KB RAM: 1.9 µA
  - Hibernate: 1.3 µA
  - SoC Off: 500 nA
  - SoC Off with Harvesting Enabled: 800 nA

RF Characteristics

- Transmit: -20 to +10 dBm
- Rx Sensitivity: -97 dBm

Interfaces

- I^2C, I^2S, SPI, UART, PWM, GPIOs
- Quad SPI
- 16-bit application ADC
- SWD for Interactive Debugging

Package Options

- 4x4 mm, 93-ball BGA (46 GPIOs)
- 5x5 mm, 40-pin QFN (up to 21 GPIOs)
- 7x7 mm, 56-pin QFN (up to 31 GPIOs)

Feature Highlights

The ATM34/e Series SoCs have been specifically designed and optimized for low-power applications. The ATM34e has a dedicated input for energy from photovoltaic and mechanical harvesting devices.

The Power Management Unit is very efficient at providing the core and I/O power for the ATM34/e, but can also be bypassed if a power source is available elsewhere in the system.

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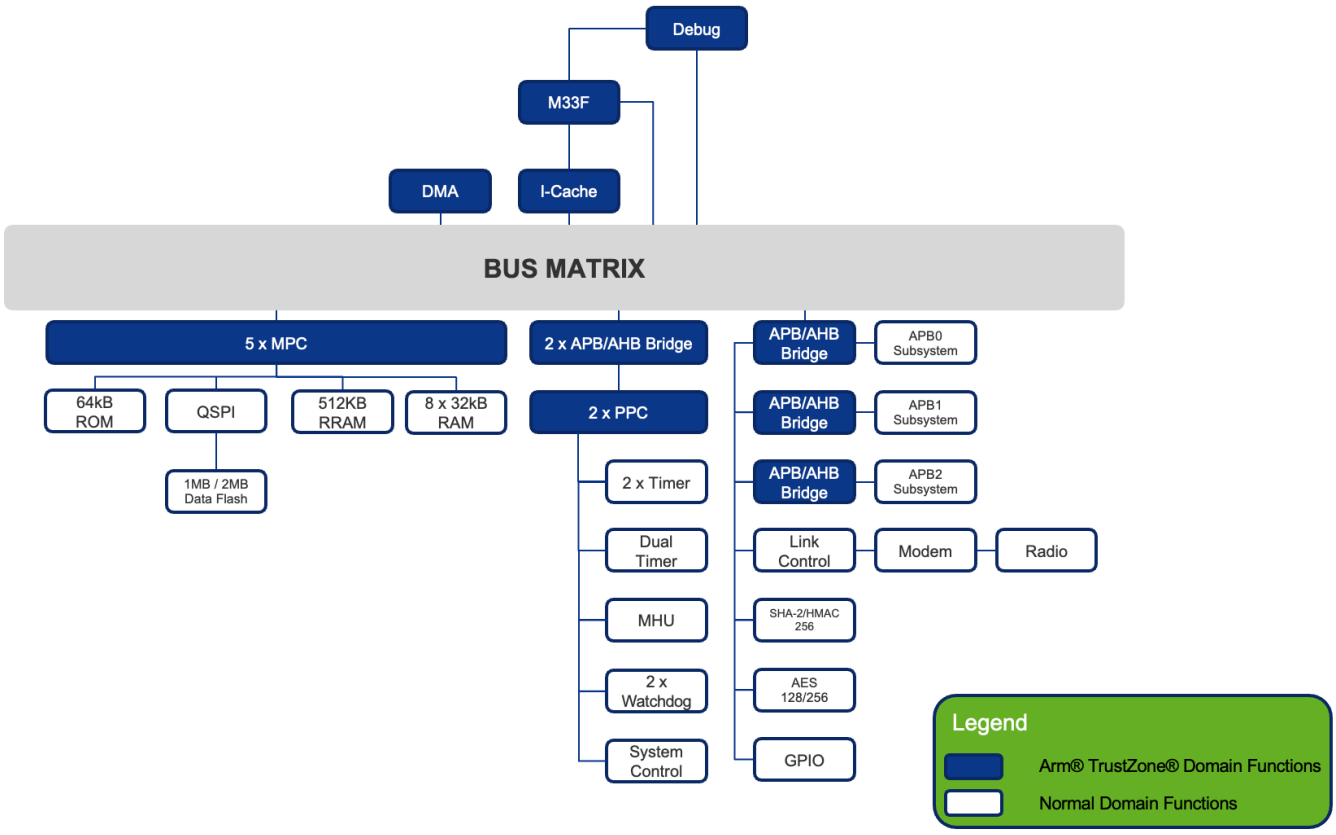
Figure 1-1 Functional Block Diagram



1.1 MCU & Memory

The ATM34/e contains a 64 MHz 32-bit ARM® Cortex®-M33F processor that is optimized for low-power operation. The processor is a little-endian, 32-bit RISC processor that implements the ARMv8-M architecture specification. It supports all Thumb-1/Thumb-2 instructions. It features four breakpoints, a serial access debug port, 117 interrupts, a single cycle multiplier, full wake-on-interrupt support, and two watchpoints. The M33F includes an IEEE-754-compliant floating-point unit (FPU). The M33F also supports ARMv8-M Digital Signal Processing (DSP) extension for audio and sensor applications. The M33F core is configured with a 4 KB instruction cache to minimize instruction fetch latency.

To reduce latency, the software can use the Direct Memory Access (DMA) core for memory-to-memory copying and for initializing blocks of memory to a constant. When it is in use, the DMA core masters the Advanced Microcontroller Bus

Architecture (AMBA) High-performance Bus (AHB) and has higher precedence than the Cortex®-M33F. When interfacing with different slaves, the DMA and MCU can operate concurrently.

The ATM34/e includes the following memory components:

- ROM: 64 KB of ROM. Core elements of the firmware are placed in ROM to add security, as well as extend application space and reduce latency.
- SRAM: The ATM34/e provides 256 KB of SRAM containing both system RAM and data RAM organized as sixteen 16 KB macros. The power state of each macro in each low-power state can be independently controlled.
- NVM: The ATM34/e is designed to provide a scalable NVM option. The base ATM34/e offers 512 KB of non-volatile memory (NVM) to store configuration, calibration data, and user application code and data. Extended memory options are available that add 1024 or 2048 KB, bringing the total NVM to 1536 or 2560 KB.

Table 1.1-1 System Memory Map

Start	Stop	Block
0x0000 0000	0x0008 FFFF	ROM + NVM [Non-secure]
0x1000 0000	0x1008 FFFF	ROM + NVM (secure]
0x0020 0000	0x002F FFFF	Extended NVM [Non-secure]
0x1020 0000	0x102F FFFF	Extended NVM [Secure]
0X2000 0000	0x2003 FFFF	SRAM [Non-secure]
0x3000 0000	0x3003 FFFF	SRAM [Secure]
0x4000 0000	0x4030 4FFF	Timers, Watchdogs, GPIO, UART, PWM, SPI, QSPI, I^2C, OTP, PMU, PSEQ, GADC, I^2S, DMA, SHA-2/HMAC 256, and AES-128/256 [Non-secure]
0x5000 0000	0x5030 4FFF	All of the above peripherals are aliased in secure space [Secure]

Non-secure and Secure address aliases are used by the Cortex processor in secure or non-secure mode. The physical mapping of the resource (memory, peripherals) to that alias is managed by the Memory Protection Controller (MPC) and Peripheral Protection Controller (PPC). Please refer to the ***Arm® TrustZone Technology for the Arm v8-M Architecture*** manual.

1.1.1 Clocks

Primary clock domains in the ATM34/e are:

- Low-power clock: 32.768 kHz crystal or an internal RC oscillator (RCOSC) for low-power operations
- RF clock: 8 MHz and 16 MHz fixed frequency clocks used by the link controller, modem, and radio subsystem
- Backplane clock: 32, 48, or 64 MHz backplane clock used by the MCU and peripherals
- I^2S: 16, 24, 32, 48, 64, 128, or 192 MHz for internal core operation
- Peripheral: 16MHz fixed frequency clock used by certain peripherals

The Real Time Counter (RTC) is a free-running counter running off the Low-power clock. It is accessible by the MCU for timestamping and only restarts when the SoC undergoes a cold start.

1.1.2 Reset

The Power Management Unit (PMU) releases the chip-wide reset once the power supplies have stabilized, which allows the SoC to cold start. There is no explicit reset pin, but the power-down (PWD) pin can be used to power cycle the ATM34/e. The MCU can reset individual peripherals and the SoC via control registers.

1.1.3 Power Modes

The ATM34/e supports five primary power states, which are Active, Retention, Hibernation, SoC Off, and Powerdown. Each primary state may have several secondary states depending on the number of active power domains and clock gating. All power states except Powerdown are managed by the power sequencer block (PSEQ).

1. **Active**: All regions of the ATM34/e are powered on. Active power can be optimized by clock-gating peripherals and/or entering these secondary states:
    - Radio Deep Sleep: The RF clock is gated while the remainder of the ATM34/e is active.
    - MCU Idle: MCU executes the Wait for Interrupt (WFI) instruction to gate internal clocks.

2. **Retention**: All or some of the 256 KB SRAM can be retained in increments of 16 KB. All register/flip-flop states needed to resume operation after waking up are retained. Digital I/Os will not lose state during Retention. The ATM34/e supports many wakeup options, including a timer expiring, activity detected on GPIOs, debug activity over SWD, and the analog comparator.

3. **Hibernation**: Powers down system memory. A minimal number of registers/flip-flops remain powered on. Digital I/Os will not lose state during Hibernation. The ATM34/e supports many wakeup options, including a timer expiring, activity detected on GPIOs, activity, debug activity over SWD, and the analog comparator. The MCU undergoes a reboot when waking from this state.

4. **SoC Off**: All digital domains, including the top-level digital domain and RTC, are powered off, but the PMU remains in an ultra-low-power state with limited functionality. The SoC undergoes a cold start when waking from this state. Wake mechanisms are limited to:

    - Special 40-bit timer
    - High-level input on P5/SOCOFF_WAKE
    - Ultra-low power analog comparator with input on either P3 or P4.

5. **Powerdown** (PWD pin asserted): All power domains, including the PMU, are completely shut off. No supplies are internally generated or maintained.

1.2 Communications Radio

1.2.1 Radio

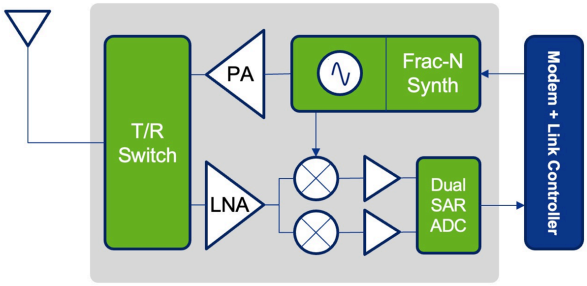
The 2.4GHz radio, shown in Figure 1.2-1, is designed to support extremely low power operation for Bluetooth Low Energy communication standards.

The radio is a single-ended shared RF interface that is internally split for receive and transmit radio communication chains.

- The receive chain includes the LNA, downconversion, mixer, IF amplifier, anti-aliasing filter, and two successive approximation analog-to-digital converters (ADC). The anti-aliasing filter, LNA, and IF amplifier are controlled by the AGC to maximize performance across the dynamic range.

- The transmit chain uses the digital direct frequency modulation of a fractional-N synthesizer to create the appropriate signal that is amplified by a power amplifier to provide the desired RF output level.

Figure 1.2-1 Radio Block Diagram



1.2.2 Modem

The modem, along with the radio, link controller, and software stack, forms a highly efficient Bluetooth Low Energy solution.

For Bluetooth Low Energy, the radio supports the 2 Mbps high-speed PHY, the 1 Mbps basic PHY, and the 500 kbps and 125 kbps Coded-PHY. The basic 1 Mbps PHY is fully compatible with Bluetooth 4.0 specifications, while the newer 2 Mbps rate can provide 2X the speed. For long-range, the Coded-PHY can provide up to 4X range. The radio architecture is also optimized for burst data transmission using Frequency-Hopping Spread Spectrum (FHSS) over 40 channels with 2 MHz spacing (3 advertising channels/37 data channels).

During the receive operation, the modem and radio are enabled prior to expected packet reception as determined by the link controller. Incoming packets are detected, tracked, processed, and forwarded to the link controller. The modem and radio receiver are turned off by the link controller at the end of a completed packet. Channel information is provided directly from the link controller to the radio without the involvement of the modem.

There is minimal involvement of the modem during transmission activity. The link controller provides the symbol bit stream, which is then shaped consistent with the signal requirements to provide the appropriate frequency deviation by the radio. Channel information and target transmit power are provided directly from the link controller to the radio.

1.2.3 Link Controller (ATLC)

The Atmosic Link Controller (ATLC) provides an interface between the MCU, modem, and tightly-coupled memory (TCM), allowing the MCU to access through the system AHB bus to the control registers and tightly coupled memory.

During transmission, the software writes the packet payload and control structures into the TCM. The link controller serializes the data into a bit stream to the modem.

During receive, the operation is reversed. Received data from the modem is processed and stored in the TCM and read by the software.

The design runs on an 8 MHz clock and is synchronous to the modem (16 MHz), AHB bus (16 MHz), and TCM (16 MHz).

1.3 Power Management Unit (PMU)

The Power Management Unit (PMU) provides the core and I/O power supplies to the ATM34/e. Harvested energy can extend the battery life or enable operation without a battery for some low-duty-cycle applications.

The PMU generates up to three power supply outputs: DVDD1P, AVDD1P, VDDIOP, and a fourth auxiliary supply, VAUX, used internally by the PMU. For more information on the board connections, refer to the *ATM34/e Hardware Design Guide*.

Table 1.3-1 PMU External Pins

Pin	Description
VBAT	Battery input Battery voltages from 1.1 V to 3.3 V can be used. Must connect to a 10 µF capacitor if VBATLI is used.
VBATLI	Lithium-ion battery input in place of VBAT Lithium-ion battery voltages from 2.7 to 4.5 V can be used. It must be connected to VBAT if not used.
VDDPA	Power supply input for the transmit power amplifier at output power levels greater than 4 dBm
VSTORE (ATM34e only)	Connection to a storage element for harvested energy Must be grounded when the harvester is not used
VHARV (ATM34e only)	Connection to an external harvesting source Must be grounded when the harvester is not used
LEXT1, LEXT2	Connections to the inductor for the PMU switching regulator
DVDD1P, AVDD1P VDDIOP	DVDD1P and AVDD1P are PMU-generated digital and analog core supply outputs VDDIOP is a PMU-generated 1.8 V I/O supply output
VAUX	PMU-generated auxiliary supply output Must be connected to a capacitor >= 10 uF
DVDD1, AVDD1	Power supply input for digital and analog core circuits

Pin	Description
VDDIO	Power supply input for digital and analog I/O circuits

The PMU provides multiple brownout interrupts to enable more reliable operation, especially when using energy harvesting.

1.3.1 PMU Configurations

The PMU must be configured correctly to ensure correct operation. The following modes of operation are supported by the PMU:

Table 1.3.1-1 PMU Configuration

PMU Configuration	VBAT Connection	VBATLI Connection	VDDIO Connection
Battery or external power supply (1.1 V - 3.3 V) with internally generated I/O supply	Battery or power supply	VBAT	VDDIOP
Battery or external power supply (1.8 V - 3.3 V) with externally generated I/O supply	Battery or power supply	VBAT	VBAT or other externally generated I/O supply (1.8 V - 3.3 V)
High Voltage battery or power source (2.7 V - 4.5 V) with internally generated I/O supply	10 µF bypass capacitor	High-voltage battery or power source	VDDIOP or other externally generated I/O supply (1.8V-3.3V)

1.4 Security

The ATM34/e offers a complete security solution, including:

- Secure boot
- Secure OTA
- Secure execution
- Key management
- Key storage
- Secure debugging

The ATM34/e has a true random number generator (TRNG), which generates a single 32-bit random number per invocation. Arbitrarily long random numbers can be achieved by repeatedly invoking this random number generator. The TRNG can also be used to seed a software hash function.

The ATM34/e also has two hardware cryptographic accelerators, AES-128/256 and SHA-2/HMAC 256, which are both accessible by software. There are provisions to load keys into the AES-128/256, where the keys themselves are not readable by any bus master.

1.5 OTP Access

The 64-bit one-time programmable memory (OTP) is used to store PMU and security configurations. The MCU can access the OTP via a controller that provides indirect access for byte reads and bit writes.

VAUX needs to be configured to 2.5 V to program OTP bits.

1.6 Timers and Interrupts

1.6.1 Wakeup Timer

The wakeup timer is a 40-bit timer based on the Low-power clock. When this timer is enabled during SoC Off mode, it will determine the SoC Off duration.

1.6.2 General Purpose Timers

There are four (4) general-purpose timer cores: Timer0, Timer1, Dual Timer, and Slow Timer. The values of the timers are readable by the MCU. Timer0, Timer1, and Dual Timer are clocked by the Peripheral clock, while the Slow Timer is clocked by the Low-power clock. All of these timers stop when the system enters a low-power state.

- Timer0 will decrement from a 32-bit load value and trigger a maskable interrupt as it transitions from 1 to 0. The reload value is loaded as the next timer value when the timer reaches 0. Additionally, there is a prescaler in front of each timer that can reduce the incoming clock by factors of 2 up to 256.
- Timer1 is identical to Timer0 with its own register space and its own interrupt.
- Dual Timer contains two timers that are independent from each other but trigger a shared maskable interrupt as either transitions from 1 to 0. Each timer counts down and can run in one-shot, periodic, or free-running mode. The timers are configurable to be either 16-bit or 32-bit. Additionally, there is a prescaler in front of each timer that can reduce the incoming clock by factors of 2 up to 256.

- Slow Timer is a 40-bit countdown timer with three programmable thresholds. Maskable interrupts are optionally asserted when the counter counts from threshold + 1 to the threshold and from 1 to 0.

1.6.3 Interrupts

The ATM34/e supports the following categories of interrupts:

- Interrupts for ARM MCU exceptions, watchdog timers, and hardware protection blocks.
- Other maskable interrupts:
  - 26 interrupts for APB peripherals
  - 4 DMA interrupts
  - 4 primary communications radio interrupts
  - 11 timer and clocking interrupts
  - 50 GPIO interrupts (93-ball BGA, 4x4 mm), 33 GPIO interrupts (56-pin QFN, 7x7 mm), 23 GPIO interrupts (40-pin QFN, 5x5 mm)

1.7 Peripherals and I/O

The following peripherals are supported by the ATM34/e:

- **GPIO**
  There are up to 46 GPIOs available in the 93-ball BGA 4x4 mm package, 31 GPIOs available in the 56-pin QFN 7x7 mm package, and up to 21 GPIOs in the 40-pin QFN 5x5 mm package. GPIOs are controlled through software-accessible registers. In addition to drive, sample, pull-up, and pull-down functions, the GPIOs can also be used to generate interrupts and to wake the ATM34/e from low-power states.
- **I^2C**
  There are two identical I^2C master cores in which the software preloads the transaction and then initiates the hardware controller. Software can either poll for completion or respond to the completion interrupt. The I^2C clock is programmable to specific frequencies between 3.9 kHz and 2 MHz and supports clock stretching.
- **Serial Peripheral Interface (SPI)**
  The ATM34/e implements two identical SPI master cores with DMA support. The software can preload the transaction, initiate it, and then either poll for completion or respond to the completion interrupt. Opcode, transaction type, data, and number of bytes are all software programmable. The hardware will serialize and sample incoming data as required by the protocol. The SPI port clock frequency is programmable to specific rates between 7.8 kHz and 8 MHz.
- **Quad Serial Peripheral Interface (QSPI)**
  There is one quad SPI master port, and it is intended to be connected to an external flash (if needed). Specific single, and quad SPI devices are supported at frequencies up to 32 MHz and can be directly memory-mapped to enable execute-in-place operation and DMA support. The core also includes a read cache to reduce latency. QSPI is available on selected packages. Please refer to Part Ordering for details.
- **UART**
  The ATM34/e implements three UART cores with flow control and DMA support. UART0 is typically used as a 4-wire host controller interface (HCI), while UART1 is typically used as a 2-wire debug interface. The baud rate is programmable to specific values between 16 to 2000000.

- **I^2S**
  The I^2S master core is designed to support an inter-IC sound bus for transporting digital audio data streams. This interface consists of:
  - SCK - system clock, bit clock, or serial clock
  - WS - word select, frame clock, or left/right clock
  - SD - serial data or data line

  Depending on how the core is configured, the module sources or sinks these interface signals. Supported operation modes are PCM mode, left-justified mode, and right-justified mode.

- **PWM**
  The PWM has eight independent pulse width modulation output channels. Each channel can operate in one of four modes:
  1. Continuous mode - The user specifies the duty cycle and the PWM channel outputs.
  2. Counting mode - The user specifies the number of times to repeat in addition to the duty cycle. This combination of duty cycle and repeat count is referred to as a frame.

  All channels support all modes of operation.

  PWM frequency ranges from 122 Hz to 8 MHz with 16-bit fields to independently control high duration and low duration.

- **Analog Comparator**
  The analog comparator provides an ultra-low power approach to sense an analog input signal from sensors and can optionally wake up the ATM34/e from a low-power state. The threshold level is programmable to one of 16 values between 150 mV and 1.65 V.

- **Application ADC**
  The General-purpose 16-bit Analog-to-Digital Converter (GADC) has a MASH 2-1 Sigma-Delta architecture, as shown in Figure 1.9-1. The 1st and 2nd Stages generate D_{out1} and D_{out2} bit streams, respectively, which are post-processed in the digital core to provide 16-bit output samples that are stored in a FIFO for software access. The GADC supports 12 physical input channels: VBAT, VSTORE, AVDD1, VBATLI, temperature, P3, P4, P5, P6, P7, P8, and P9, of which P4/P5 and P6/P7 can also be configured as differential inputs.

For the maximum number of general-purpose peripherals supported in each package (GADC, UART, QSPI, SPI, I^2S, I^2C, PWM), please refer to Part Ordering.

1.8 Pin Multiplexing

The 46 programmable I/O pins of the 4x4 mm 93-ball BGA package may be programmed and connected to multiple functional signals. The 7x7 mm 56-pin QFN package supports 31 programmable pins, and the 5x5 mm 40-pin QFN package supports 21 programmable pins.

In addition, each of these I/O pins can be configured to enable an internal pull-up or pull-down as well as one of 4 drive strength levels. A pin multiplexing tool provided in the SDK can be used to program the I/Os to the desired function.

2 Electrical Specification

All parameters' typical values are based on a 3 V supply at 25 °C unless otherwise specified, and if specified, min/max values are based on the worst-case process variation, voltage, and ambient temperature conditions. Radio parameters are measured using a conducted configuration.

Table 2-1 Maximum Electrical Ratings[1]

Symbol	Parameter	Min	Typ	Max	Unit
VBAT	Battery voltage	-0.2		3.9	V
VBATLI	Lithium-ion battery supply	2.4		6.0	V
	Charge ramp rate			15	V/s
VDDPA	PA supply	-0.2		3.6	V
VSTORE	Storage element	-0.2		3.6	V
VDDIO	I/O supply	-0.2		3.6	V
VAUX	PMU Auxiliary Supply	-0.2		3.6	V
VIO	I/O pin (VDDIO > 3.4 V) I/O pin (VDDIO <= 3.4 V)	-0.2 -0.2		3.6 VDDIO+0.2	V
VRF	RF I/O pin as input			10	dBm
ESD_{HBM}	ESD HBM			2000	V
ESD_{CDM}	ESD CDM			500	V
T_{STORE}	Storage Temperature	-40		125	°C

[1] Maximum ratings represent the highest levels to which the chip can be exposed for a short duration without incurring permanent damage. Prolonged exposure to these absolute maximum ratings may compromise the reliability of the device.

Table 2-2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDDIO	I/O supply	1.7	1.8	3.465	V
VBAT	Battery supply	1.1		3.6	V
VBATLI	Lithium-ion battery supply	2.7		4.5	V
VDDPA	PA supply	0.05	1.8	3.465	V
VAUX	PMU Auxiliary Supply	2.375	3.3	3.465	V
VIO	I/O pin	0		VDDIO+0.2	V
	Crystal (Tolerance + Stability) - 16.000 MHz	-50		50	ppm
	Crystal (Tolerance + Stability) - 32.768 kHz	-500		500	ppm
TA	Operating (Ambient) Temperature	-40	25	105[2]	°C

[2] Maximum TA for ATM3405 4x4 mm BGA package is 85°C

Table 2-3 Radio Transceiver Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Frequency		2.402		2.480	GHz
Rx sensitivity	37-byte packets, clean Tx				
	125 kbps		-103		dBm
	500 kbps		-100		dBm
	1 Mbps		-97		dBm
	2 Mbps		-95		dBm
	255-byte packets, dirty Tx				
	125 kbps		-101		dBm
	500 kbps		-98		dBm
	1 Mbps		-95		dBm
	2 Mbps		-92		dBm
Rx Carrier-to-Interferer	1 Mbps, Co-channel		15	21	dB
	1 Mbps, Adjacent 1 MHz		3	15	dB
	1 Mbps, Adjacent 2 MHz		-35	-17	dB
	1 Mbps, Adjacent 3 MHz		-40	-27	dB
Tx output power		-20		10	dBm
Tx power accuracy			+/-1.5		dB
Tx spectral mask	1 Mbps, 2 MHz offset			-20	dBm
	1 Mbps, > 3 MHz offset			-30	dBm
RSSI resolution			1		dB
RSSI accuracy	-90 to -20 dBm		+/-2		dB

Table 2-4 PMU Characteristics[3]

Parameter	Conditions	Min	Typ	Max	Unit
AVDD1P Output Voltage		0.95	1.0	1.155	V
DVDD1P Output Voltage		0.76	1.1	1.155	V
VDDIOP Output Voltage		1.71	1.8	1.89	V
VAUX Output Voltage		2.375	3.3	3.465	V

Table 2-5 GPIO Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Input VIH		VDDIO * 0.7			V
Input VIL				VDDIO * 0.3	V
Drive Strength, push-pull high	VIO=VDDIO-0.3V				
	VDDIO = 3.3 V, PDSN=0		21		mA
	VDDIO = 3.3 V, PDSN=1		15		mA
	VDDIO = 3.3 V, PDSN=2		11		mA
	VDDIO = 3.3 V, PDSN=3		4		mA
	VDDIO = 1.8 V, PDSN=0		14		mA
	VDDIO = 1.8 V, PDSN=1		9		mA
	VDDIO = 1.8 V, PDSN=2		7		mA
	VDDIO = 1.8 V, PDSN=3		2		mA
Drive Strength, push-pull low	VIO is 0.3V				
	VDDIO = 3.3 V, PDSN=0		27		mA
	VDDIO = 3.3 V, PDSN=1		18		mA
	VDDIO = 3.3 V, PDSN=2		14		mA
	VDDIO = 3.3 V, PDSN=3		5		mA
	VDDIO = 1.8 V, PDSN=0		18		mA
	VDDIO = 1.8 V, PDSN=1		12		mA

[3] Values in this table do not include the effects of switching regulator ripple. The typical values represent default values that may be adjusted by software.

Parameter	Conditions	Min	Typ	Max	Unit
	VDDIO = 1.8 V, PDSN=2 VDDIO = 1.8 V, PDSN=3		9 3		mA mA
Pull-up/down Resistance			145		kΩ

Table 2-6 Application ADC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
ADC Sample Resolution			16		bits
Programmable Gain	0.125, 0.25, 0.5, 1	0.125		1	
Power Consumption (VBAT current at 3 V)	VBATLI channel All other channels		220 200		µA
Measurement duration	2 MHz, 128-sample averaging 2 MHz, 32-sample averaging		8 2		ms
Effective Number of Bits[4]	Differential channel, Gain = 0.25, 2 MHz, 128-sample averaging Differential channel, Gain = 0.25, 2 MHz, 32-sample averaging Single-ended channel, Gain = 0.25, 2 MHz, 128-sample averaging Single-ended channel, Gain = 0.25, 2 MHz, 32-sample averaging		12.5 12.3 11.5 11.4		bits
Signal to Noise and Distortion Ratio[4]	Differential channel, Gain = 0.25, 2 MHz, 128-sample averaging Differential channel, Gain = 0.25, 2 MHz, 32-sample averaging		77.0 75.8		dB

[4] The relationship between ENOB and SNDR is specified according to the standard ENOB calculator formula: ENOB = (SNDR - 1.76)/6.02

Parameter	Conditions	Min	Typ	Max	Unit
	Single-ended channel, Gain = 0.25, 2 MHz, 128-sample averaging		71.1		
	Single-ended channel, Gain = 0.25, 2 MHz, 32-sample averaging		70.5		
Total Harmonic Distortion	Differential channel, Gain = 0.25, 2 MHz, 128-sample averaging		-91		dB
	Differential channel, Gain = 0.25, 2 MHz, 32-sample averaging		-87		
	Single-ended channel, Gain = 0.25, 2 MHz, 128-sample averaging		-88		
	Single-ended channel, Gain = 0.25, 2 MHz, 32-sample averaging		-85		
Spurious Free Dynamic Range	Differential channel, Gain = 0.25, 2 MHz, 128-sample averaging		89		dB
	Differential channel, Gain = 0.25, 2 MHz, 32-sample averaging		88		
	Single-ended channel, Gain = 0.25, 2 MHz, 128-sample averaging		84		
	Single-ended channel, Gain = 0.25, 2 MHz, 32-sample averaging		83		
Integral Nonlinearity			+/- 0.65		LSB12
Differential Nonlinearity			+/- 0.75		LSB12
Gain Error			+/- 0.6		%
Offset Error			+/- 2		LSB12

Table 2-7 Radio Power Consumption

Radio Power Consumption **VBAT current at 3 V based on AVDD1 current, assuming 80% PMU efficiency**					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Radio Receiver Rx	Sensitivity at -97 dBm		0.95		mA
Radio Transmitter Tx	Output power at 0 dBm		2.5		mA

Table 2-8 SoC Power Consumption (3 V VBAT)

SoC Power Consumption **VBAT current at 3 V with an internally generated I/O supply** (Active RX and Active Tx SoC Power Consumption includes Radio Power Consumption)					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Active RX	Sensitivity at: -97 dBm		 1.5		 mA
Active TX	Output power at: -20 dBm -10 dBm -8 dBm -6 dBm -4 dBm -2 dBm 0 dBm +2 dBm +4 dBm +6 dBm +8 dBm +10 dBm		 1.2 1.6 1.8 2.1 2.3 2.6 3.0 3.6 4.2 8.5 10.0 12.5		 mA mA mA mA mA mA mA mA mA mA mA mA
MCU Active (32 MHz)	Executing CoreMark from RAM at 32 MHz		1.5		mA
MCU Active (64 MHz)	Executing CoreMark from RAM at 64 MHz		3.0		mA

MCU Idle + Radio Deep Sleep			0.3		mA
Retention	0 KB SRAM 32 KB SRAM 128 KB SRAM 256 KB SRAM		1.8 1.9 2.1 2.4		µA µA µA µA
Hibernation			1.3		µA
SoC Off with Harvesting Enabled			800		nA
SoC Off with Analog Comparator enabled			650		nA
SoC Off			500		nA
Powerdown	PWD pin asserted		120		nA

Table 2-9 SoC Power Consumption (4.2 V VBATLI)

SoC Power Consumption

VBATLI current at 4.2 V with an internally generated I/O supply

(Active RX and Active Tx SoC Power Consumption includes Radio Power Consumption)

Parameter	Conditions	Min	Typ	Max	Unit
Active RX	Sensitivity at: -97 dBm		 1.5		 mA
Active TX	Output power at: -20 dBm -10 dBm -8 dBm -6 dBm -4 dBm -2 dBm 0 dBm +2 dBm +4 dBm		 1.2 1.5 1.6 1.9 2.1 2.4 2.8 3.5 4.1		 mA mA mA mA mA mA mA mA mA

	+6 dBm +8 dBm +10 dBm		7.5 9.5 11.5		mA mA mA
MCU Active (32 MHz)	Executing CoreMark from RAM at 32 MHz		1.6		mA
MCU Active (64 MHz)	Executing CoreMark from RAM at 64 MHz		3.2		mA
MCU Idle + Radio Deep Sleep			0.4		mA
Retention	0 KB SRAM 32 KB SRAM 128 KB SRAM 256 KB SRAM		1.9 2.0 2.2 2.5		µA µA µA µA
Hibernation			1.3		µA
SoC Off with Harvesting Enabled			1000		nA
SoC Off with Analog Comparator enabled			850		nA
SoC Off			700		nA
Powerdown	PWD pin asserted		120		nA

Table 2-10 Energy Harvesting (ATM34e only)

Symbol	Parameter	Min	Typ	Max	Unit
VHARV	Cold Start Voltage		0.5		V
	Steady State Regulated Voltage	0.4		3.3	V
	Input Current @ 3 V	1		10,000	µA
VSTORE	Voltage			3.3	V

Table 2-11 NVM Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VDDIO		1.62	1.8	3.6	V
Endurance		10000			Cycles
Data Retention		10			Years
Read Cycle	VDDIO Current @ 1.8 V Duration (4 bytes at 32 MHz)		0.35 0.2		mA µs
Write Cycle Pattern: 0x55 -> 0xaa	VDDIO Current @ 1.8 V Duration (4 bytes at 32 MHz)		4.6 150		mA µs

Table 2-12 Extended NVM Characteristics

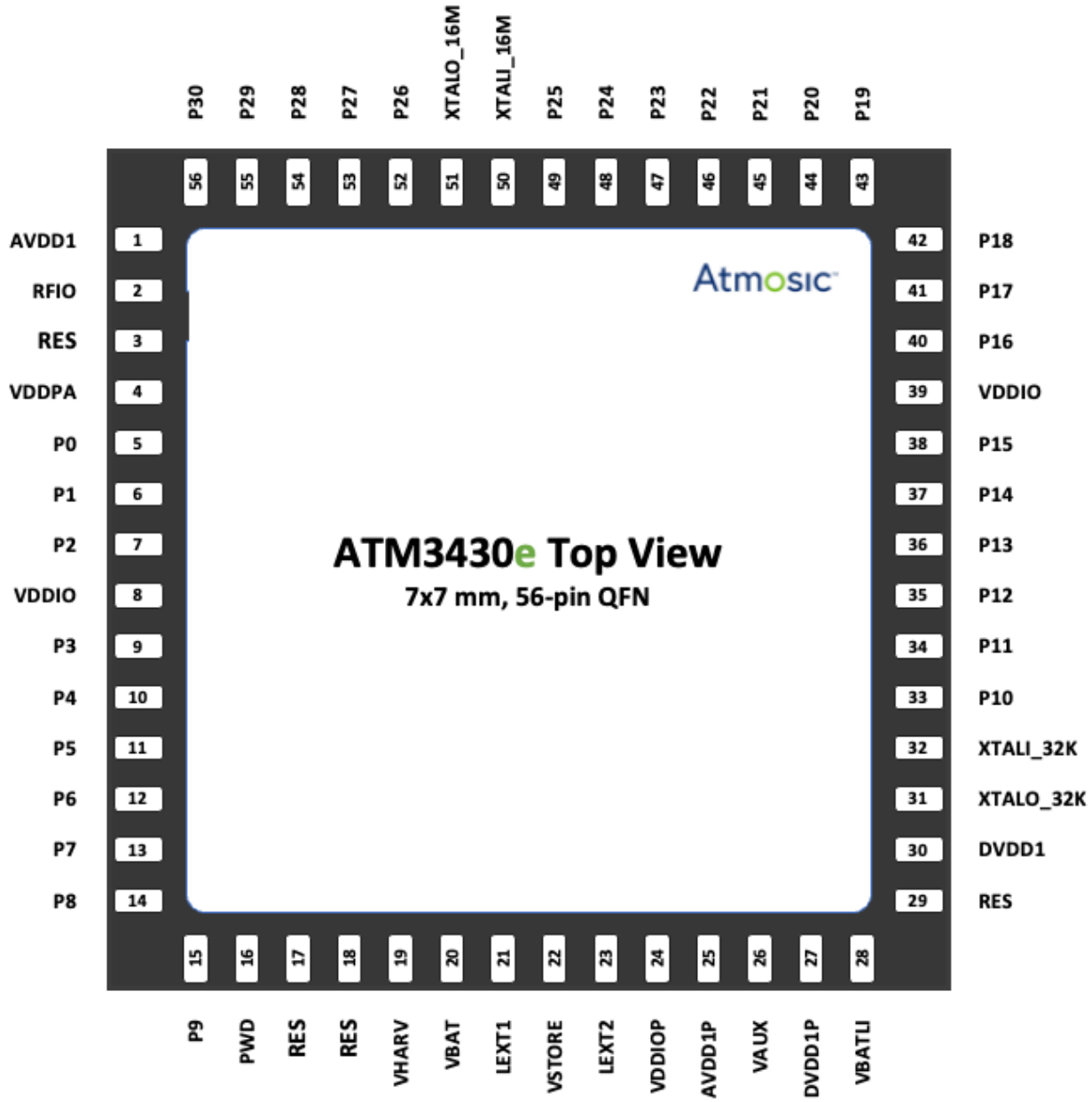
Symbol	Parameter	Min	Typ	Max	Unit
VDDIO		1.62	1.8	3.6	V
Endurance		100000			Cycles
Data Retention		20			Years
Read Cycle	VDDIO Current @ 1.8 V Duration (4 bytes at 32 MHz)		2.0 1.0		mA µs
Write Cycle	VDDIO Current @ 1.8 V Duration (256 bytes at 32 MHz)		2.7 1.7		mA ms

3 Pinout Description

3.1 ATM3430e 7x7 mm, 56-pin QFN Pinout

The ATM3430e 7x7 mm version is packaged in a No Lead Quad Flat Package (QFN). The pin assignment is shown in Table 3.1-1. All pins are on the bottom side of the package.

Figure 3.1-1 ATM3430e 7x7 mm, 56-pin QFN Pinout (Top View)



Pin Type Definitions	
Pin Type	**Definition**
I/O	Signal Input or Output
RF	Radio Frequency
PWR	Power supply
A	Analog
R	Reserved
NC	No connection, must be open
GND	Ground

Table 3.1-1 ATM3430/e 7x7 mm, 56-pin QFN Pin Description

ATM3430/e 7x7 mm, 56-pin QFN Pin Description			
Pin Number	**Name**	**Type**	**Description**
1	AVDD1	PWR	Analog and RF core power supply
2	RFIO	RF	2.4 GHz Single-ended RF I/O for the Bluetooth Low Energy radio
3	RES	R	Reserved, must tie to ground
4	VDDPA	I/O	PA power supply
5	P0	I/O	Programmable Digital I/O and SWDCLK
6	P1	I/O	Programmable Digital I/O and SWDIO
7	P2	I/O	Programmable Digital I/O
8	VDDIO	PWR	Digital and Analog I/O Power Supply
9	P3	I/O	Programmable Digital I/O or Analog Input
10	P4	I/O	Programmable Digital I/O or Analog Input
11	P5	I/O	Programmable Digital I/O or Analog Input and SOCOFF_WAKE
12	P6	I/O	Programmable Digital I/O or Analog Input
13	P7	I/O	Programmable Digital I/O or Analog Input
14	P8	I/O	Programmable Digital I/O or Analog Input

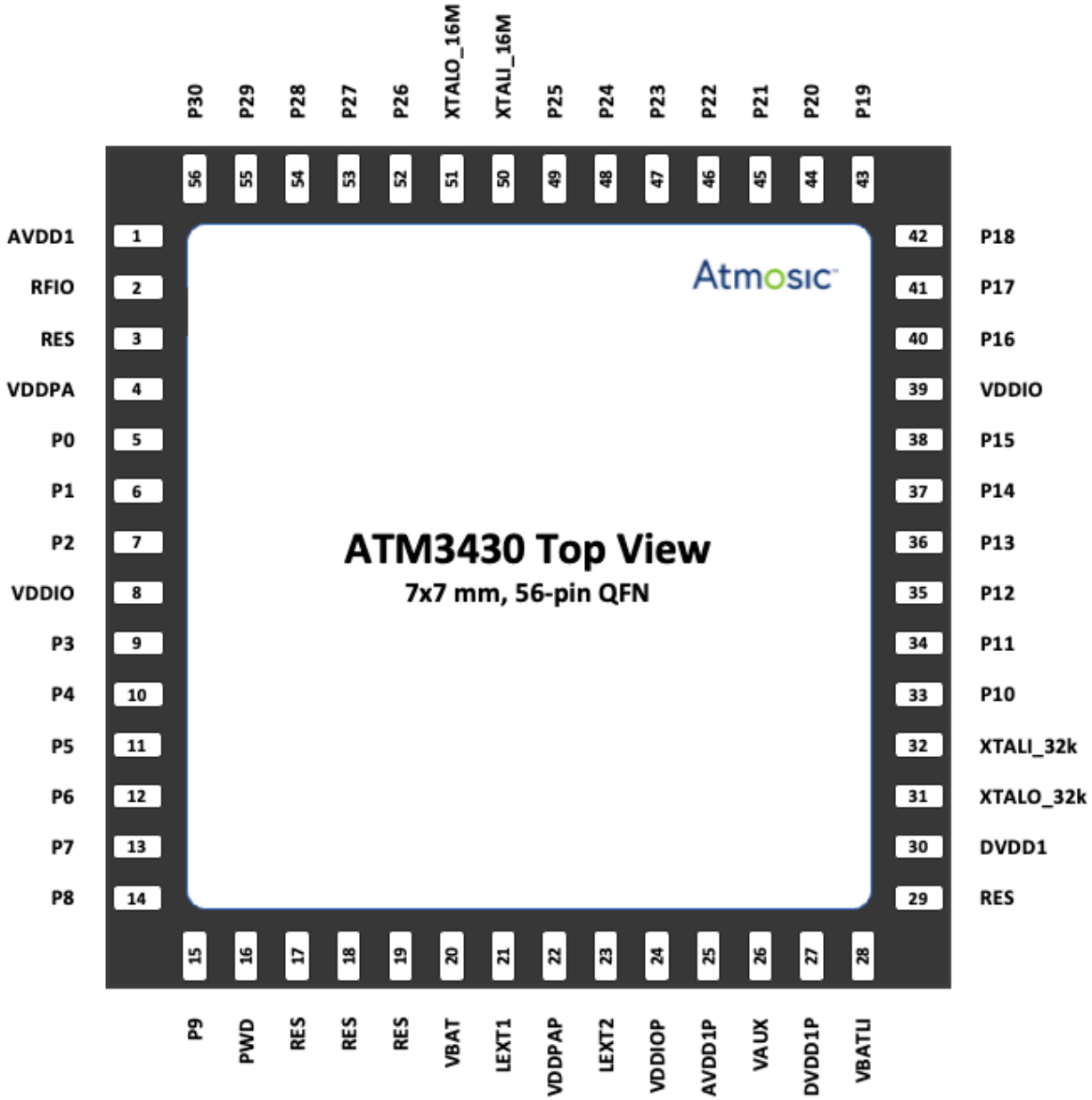
15	P9	I/O	Programmable Digital I/O or Analog Input
16	PWD	I/O	Power Down Input (Active High)
17	HARV_INP	R	Reserved, must tie to ground
18	HARV_INN	R	Reserved, must tie to ground
19	VHARV	A	Input for external harvesting source. Should be grounded if energy harvesting is not used
20	VBAT	PWR	Battery supply, must connect to a 10 µF capacitor if VBATLI is used
21	LEXT1	A	Switcher Inductor
22	VSTORE	PWR	Storage node for energy harvesting
23	LEXT2	A	Switcher Inductor
24	VDDIOP	PWR	I/O power supply generated by PMU
25	AVDD1P	PWR	Analog core power supply generated by the PMU
26	VAUX	PWR	Reserved for PMU internal use, must connect to a 10 µF capacitor
27	DVDD1P	PWR	Digital core power supply generated by PMU
28	VBATLI	PWR	Lithium-ion battery input in place of VBAT, VBATLI must be connected to VBAT if not used
29	RES	R	Reserved, must tie to ground
30	DVDD1	PWR	Digital core power supply
31	XTALO_32k	A	32.768 kHz crystal oscillator output
32	XTALI_32k	A	32.768 kHz crystal oscillator input
33	P10	I/O	Programmable Digital I/O
34	P11	I/O	Programmable Digital I/O
35	P12	I/O	Programmable Digital I/O
36	P13	I/O	Programmable Digital I/O
37	P14	I/O	Programmable Digital I/O
38	P15	I/O	Programmable Digital I/O
39	VDDIO	PWR	Digital and Analog I/O Power Supply
40	P16	I/O	Programmable Digital I/O
41	P17	I/O	Programmable Digital I/O
42	P18	I/O	Programmable Digital I/O

43	P19	I/O	Programmable Digital I/O
44	P20	I/O	Programmable Digital I/O
45	P21	I/O	Programmable Digital I/O
46	P22	I/O	Programmable Digital I/O
47	P23	I/O	Programmable Digital I/O
48	P24	I/O	Programmable Digital I/O
49	P25	I/O	Programmable Digital I/O, a weak pull low is required during the MCU boot
50	XTALI_16M	A	16 MHz crystal oscillator input
51	XTALO_16M	A	16 MHz crystal oscillator output
52	P26	I/O	Programmable Digital I/O
53	P27	I/O	Programmable Digital I/O
54	P28	I/O	Programmable Digital I/O
55	P29	I/O	Programmable Digital I/O
56	P30	I/O	Programmable Digital I/O
EPAD	VSS	GND	Ground supply for all circuits. The 56-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS.

3.2 ATM3430 7x7 mm, 56-pin QFN Pinout

The ATM3430 7x7 mm version is packaged in a No Lead Quad Flat Package (QFN). The pin assignment is shown in Table 3.2-1. All pins are on the bottom side of the package.

Figure 3.2-1 ATM3430 7x7 mm, 56-pin QFN Pinout (Top View)



Pin Type Definitions	
Pin Type	**Definition**
I/O	Signal Input or Output
RF	Radio Frequency
PWR	Power supply
A	Analog
R	Reserved
NC	No connection, must be open
GND	Ground

Table 3.2-1 ATM3430 7x7 mm, 56-pin QFN Pin Description

ATM3430 7x7 mm, 56-pin QFN Pin Description			
Pin Number	**Name**	**Type**	**Description**
1	AVDD1	PWR	Analog and RF core power supply
2	RFIO	RF	2.4 GHz Single-ended RF I/O for the Bluetooth Low Energy radio
3	RES	R	Reserved, must tie to ground
4	VDDPA	I/O	PA power supply
5	P0	I/O	Programmable Digital I/O and SWDCLK
6	P1	I/O	Programmable Digital I/O and SWDIO
7	P2	I/O	Programmable Digital I/O
8	VDDIO	PWR	Digital and Analog I/O Power Supply
9	P3	I/O	Programmable Digital I/O or Analog Input
10	P4	I/O	Programmable Digital I/O or Analog Input
11	P5	I/O	Programmable Digital I/O or Analog Input and SOCOFF_WAKE
12	P6	I/O	Programmable Digital I/O or Analog Input
13	P7	I/O	Programmable Digital I/O or Analog Input
14	P8	I/O	Programmable Digital I/O or Analog Input

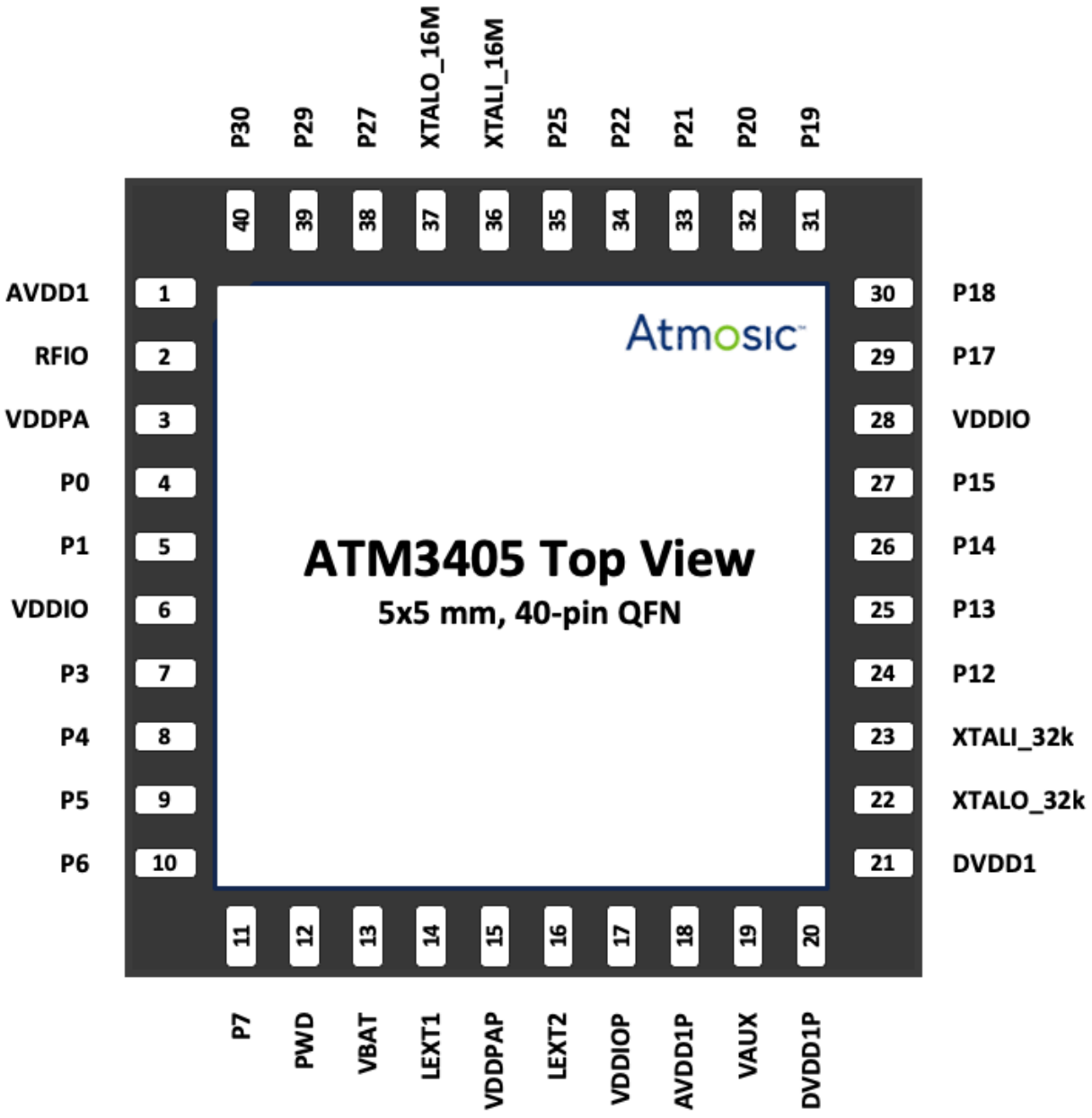
15	P9	I/O	Programmable Digital I/O or Analog Input
16	PWD	I/O	Power Down Input (Active High)
17	RES	R	Reserved, must tie to ground
18	RES	R	Reserved, must tie to ground
19	RES	R	Reserved, must tie to ground
20	VBAT	PWR	Battery supply, must connect to a 10 µF capacitor if VBATLI is used
21	LEXT1	A	Switcher Inductor
22	VDDPAP	R	Must connect to ground
23	LEXT2	A	Switcher Inductor
24	VDDIOP	PWR	I/O power supply generated by PMU
25	AVDD1P	PWR	Analog core power supply generated by the PMU
26	VAUX	PWR	Reserved for PMU internal use, must connect to a 10 µF capacitor
27	DVDD1P	PWR	Digital core power supply generated by PMU
28	VBATLI	PWR	Lithium-ion battery input in place of VBAT, VBATLI must be connected to VBAT if not used
29	RES	R	Reserved, must tie to ground
30	DVDD1	PWR	Digital core power supply
31	XTALO_32k	A	32.768 kHz crystal oscillator output
32	XTALI_32k	A	32.768 kHz crystal oscillator input
33	P10	I/O	Programmable Digital I/O
34	P11	I/O	Programmable Digital I/O
35	P12	I/O	Programmable Digital I/O
36	P13	I/O	Programmable Digital I/O
37	P14	I/O	Programmable Digital I/O
38	P15	I/O	Programmable Digital I/O
39	VDDIO	PWR	Digital and Analog I/O Power Supply
40	P16	I/O	Programmable Digital I/O
41	P17	I/O	Programmable Digital I/O
42	P18	I/O	Programmable Digital I/O

43	P19	I/O	Programmable Digital I/O
44	P20	I/O	Programmable Digital I/O
45	P21	I/O	Programmable Digital I/O
46	P22	I/O	Programmable Digital I/O
47	P23	I/O	Programmable Digital I/O
48	P24	I/O	Programmable Digital I/O
49	P25	I/O	Programmable Digital I/O, a weak pull low is required during the MCU boot
50	XTALI_16M	A	16 MHz crystal oscillator input
51	XTALO_16M	A	16 MHz crystal oscillator output
52	P26	I/O	Programmable Digital I/O
53	P27	I/O	Programmable Digital I/O
54	P28	I/O	Programmable Digital I/O
55	P29	I/O	Programmable Digital I/O
56	P30	I/O	Programmable Digital I/O
EPAD	VSS	GND	Ground supply for all circuits. The 56-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS.

3.3 ATM3405 5x5 mm, 40-pin QFN Pinout

The ATM3405 5x5 mm versions (ATM3405-5PCAQK, ATM3405-5WCAQK) are packaged in a No Lead, 40-pin Quad Flat Package (QFN). The pin assignment is shown in Table 3.3-1. All pins are on the bottom side of the package.

Figure 3.3-1 ATM3405 5x5 mm, 40-pin QFN Pinout (Top View)



Pin Type Definitions	
Pin Type	**Definition**
I/O	Signal Input Output
RF	Radio Frequency
PWR	Power supply
A	Analog
R	Reserved
NC	No connection, must be open
GND	Ground

Table 3.3-1 ATM3405 5x5 mm, 40-pin QFN Pin Description

ATM3405 5x5 mm, 40-pin QFN Pin Description			
Pin Number	**Name**	**Type**	**Description**
1	AVDD1	PWR	Analog core power supply
2	RFIO	RF	2.4 GHz Single-ended RF I/O for Bluetooth radio
3	VDDPA	PWR	PA power supply
4	P0	I/O	Programmable Digital I/O and SWDCLK
5	P1	I/O	Programmable Digital I/O and SWDIO
6	VDDIO	I/O	Digital and Analog I/O Power Supply
7	P3	I/O	Programmable Digital I/O or Analog Input
8	P4	I/O	Programmable Digital I/O or Analog Input
9	P5	I/O	Programmable Digital I/O or Analog Input and SOCOFF_WAKE
10	P6	I/O	Programmable Digital I/O or Analog Input
11	P7	I/O	Programmable Digital I/O or Analog Input
12	PWD	I/O	Power Down Input (Active High)
13	VBAT	PWR	Battery supply
14	LEXT1	A	Switcher Inductor
15	VDDPAP	R	Must connect to ground
16	LEXT2	A	Switcher Inductor
17	VDDIOP	PWR	I/O power supply generated by PMU
18	AVDD1P	PWR	Analog and RF core power supply generated by the PMU
19	VAUX	PWR	Reserved for PMU internal use, must connect to a 10 µF capacitor
20	DVDD1P	PWR	Digital core power supply generated by PMU
21	DVDD1	PWR	Digital core power supply
22	XTALO_32k	A	32.768 kHz crystal oscillator output

23	XTALI_32K	A	32.768 kHz crystal oscillator input
24	P12	I/O	Programmable Digital I/O
25	P13	I/O	Programmable Digital I/O
26	P14	I/O	Programmable Digital I/O
27	P15	I/O	Programmable Digital I/O
28	VDDIO	I/O	Digital and Analog I/O Power Supply
29	P17	I/O	Programmable Digital I/O
30	P18	I/O	Programmable Digital I/O
31	P19	I/O	Programmable Digital I/O
32	P20	I/O	Programmable Digital I/O
33	P21	I/O	Programmable Digital I/O
34	P22	I/O	Programmable Digital I/O
35	P25	I/O	Programmable Digital I/O, a weak pull low is required during the MCU boot
36	XTALI_16M	A	16 MHz crystal oscillator input
37	XTALO_16M	A	16 MHz crystal oscillator output
38	P27	I/O	Programmable Digital I/O
39	P29	I/O	Programmable Digital I/O
40	P30	I/O	Programmable Digital I/O
EPAD	VSS	GND	Ground supply for all circuits. The 40-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS.

3.4 ATM3405 4x4 mm, 93-ball BGA Pinout

The ATM3405 4x4 mm BGA version is packaged in a No Lead, 93-ball Ball Grid Array Flat Package (BGA). The pin assignment is shown in Table 3.4-1. All pins are on the bottom side of the package.

Figure 3.4-1 **ATM3405 4x4 mm, 93-ball BGA Pinout (Top View)**

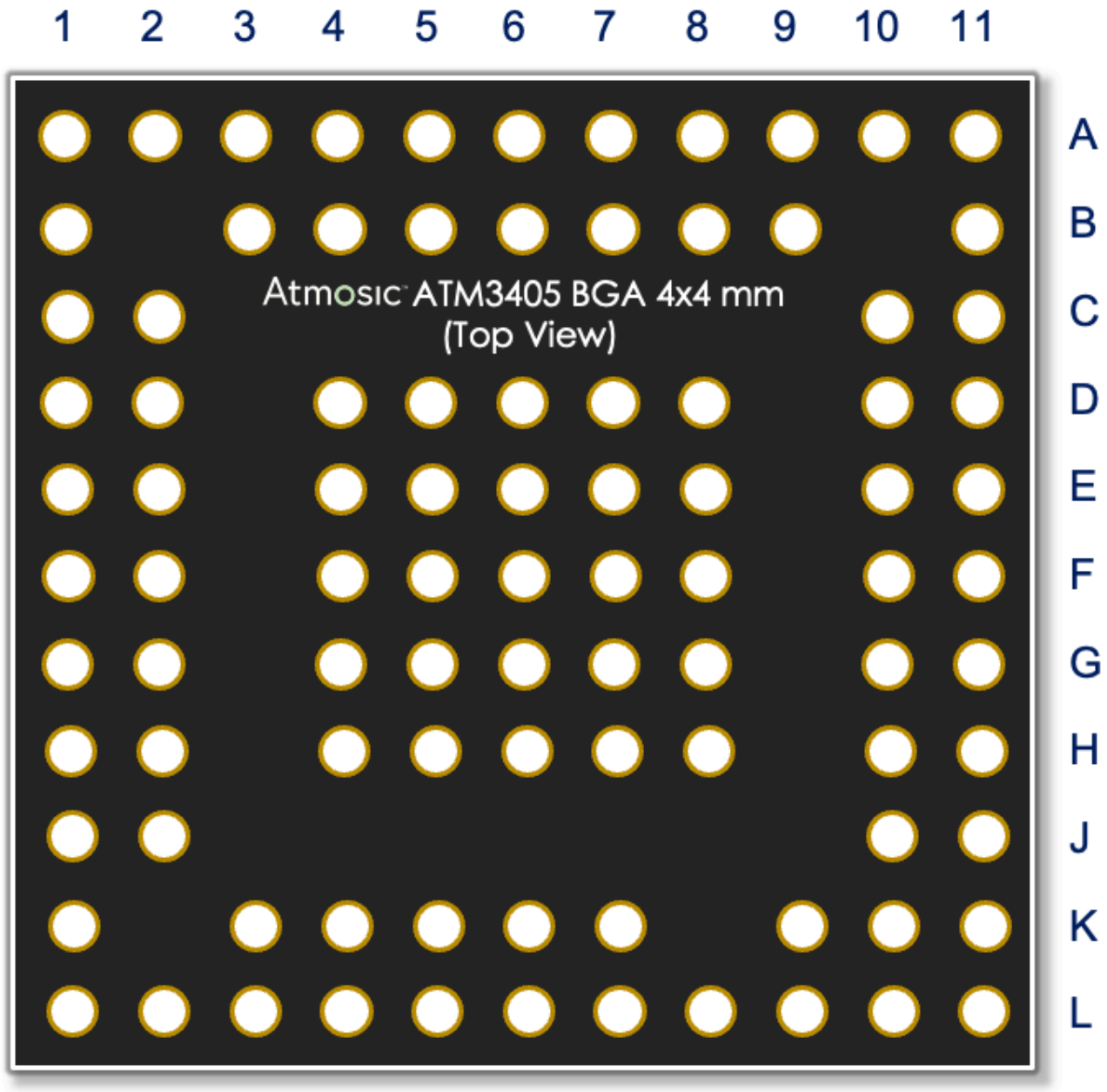
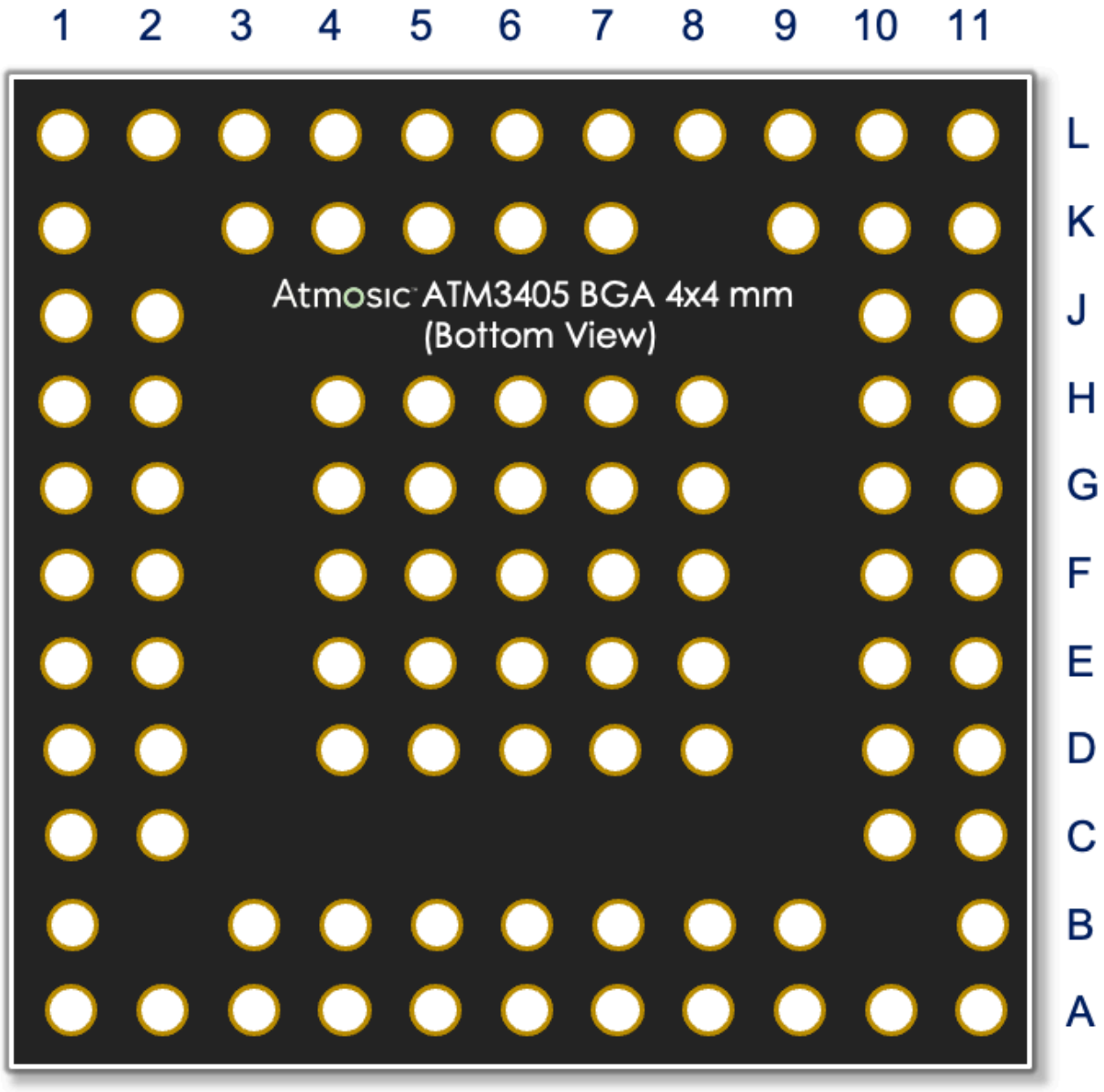


Figure 3.4-2 **ATM3405 4x4 mm, 93-ball BGA Pinout (Bottom View)**



Pin Type Definitions	
Pin Type	**Definition**
I/O	Signal Input Output
RF	Radio Frequency
PWR	Power supply
A	Analog
R	Reserved
NC	No connection, must be open
GND	Ground

Table 3.4-1 ATM3405 4x4 mm, 93-ball BGA Pin Description

ATM3405 4x4 mm, 93-ball BGA Description			
Ball Number	**Name**	**Type**	**Description**
A1	RFIO	RF	2.4 GHz Single-ended RF I/O for Bluetooth radio
A2	AVDD1	PWR	Analog core power supply
A3	P30	I/O	Programmable Digital I/O
A4	P28	I/O	Programmable Digital I/O
A5	XTALO_16M	A	16 MHz crystal oscillator output
A6	XTALI_16M	A	16 MHz crystal oscillator input
A7	P24	I/O	Programmable Digital I/O
A8	P23	I/O	Programmable Digital I/O
A9	P21	I/O	Programmable Digital I/O
A10	P19	I/O	Programmable Digital I/O
A11	P18	I/O	Programmable Digital I/O
B1	VDDPA	PWR	PA power supply
B3	P29	I/O	Programmable Digital I/O
B4	P27	I/O	Programmable Digital I/O
B5	P26	I/O	Programmable Digital I/O
B6	P25	I/O	Programmable Digital I/O, a weak pull low is required during the MCU boot
B7	P39	I/O	Programmable Digital I/O
B8	P22	I/O	Programmable Digital I/O
B9	P20	I/O	Programmable Digital I/O
B11	P17	I/O	Programmable Digital I/O
C1	P1	I/O	Programmable Digital I/O and SWDIO

C2	P0	I/O	Programmable Digital I/O and SWDCLK
C10	P38	I/O	Programmable Digital I/O
C11	VDDIO	PWR	Digital and Analog I/O Power Supply
D1	P41	I/O	Programmable Digital I/O
D2	P2	I/O	Programmable Digital I/O
D4	VSS	GND	Ground supply for all circuits
D5	VSS	GND	Ground supply for all circuits
D6	VSS	GND	Ground supply for all circuits
D7	VSS	GND	Ground supply for all circuits
D8	VSS	GND	Ground supply for all circuits
D10	P16	I/O	Programmable Digital I/O
D11	P15	I/O	Programmable Digital I/O
E1	P42	I/O	Programmable Digital I/O
E2	P48	I/O	Programmable Digital I/O
E4	VSS	GND	Ground supply for all circuits
E5	VSS	GND	Ground supply for all circuits
E6	VSS	GND	Ground supply for all circuits
E7	VSS	GND	Ground supply for all circuits
E8	VSS	GND	Ground supply for all circuits
E10	P37	I/O	Programmable Digital I/O
E11	P14	I/O	Programmable Digital I/O
F1	P43	I/O	Programmable Digital I/O
F2	P49	I/O	Programmable Digital I/O
F4	VSS	GND	Ground supply for all circuits
F5	VSS	GND	Ground supply for all circuits
F6	VSS	GND	Ground supply for all circuits
F7	VSS	GND	Ground supply for all circuits
F8	VSS	GND	Ground supply for all circuits
F10	NC	I/O	No Connection
F11	P13	I/O	Programmable Digital I/O
G1	P44	I/O	Programmable Digital I/O
G2	P50	I/O	Programmable Digital I/O
G4	VSS	GND	Ground supply for all circuits
G5	VSS	GND	Ground supply for all circuits
G6	VSS	GND	Ground supply for all circuits
G7	VSS	GND	Ground supply for all circuits
G8	VSS	GND	Ground supply for all circuits
G10	NC	I/O	No Connection
G11	P12	I/O	Programmable Digital I/O
H1	P45	I/O	Programmable Digital I/O
H2	P51	I/O	Programmable Digital I/O
H4	VSS	GND	Ground supply for all circuits

H5	VSS	GND	Ground supply for all circuits
H6	VSS	GND	Ground supply for all circuits
H7	VSS	GND	Ground supply for all circuits
H8	VSS	GND	Ground supply for all circuits
H10	P11	I/O	Programmable Digital I/O
H11	P10	I/O	Programmable Digital I/O
J1	P46	I/O	Programmable Digital I/O
J2	P47	I/O	Programmable Digital I/O
J10	P40	I/O	Programmable Digital I/O
J11	XTALI_32K	A	32.768 kHz crystal oscillator input
K1	P3	I/O	Programmable Digital I/O or Analog Input
K3	P6	I/O	Programmable Digital I/O or Analog Input
K4	P8	I/O	Programmable Digital I/O or Analog Input
K5	PWD	I/O	Power Down Input (Active High)
K6	VBAT	PWR	Battery supply
K7	VDDPAP	R	Must connect to ground
K9	VAUX	PWR	Reserved for PMU internal use, must connect to a 10 µF capacitor
K10	DVDD1	PWR	Digital core power supply
K11	XTALO_32k	A	32.768 kHz crystal oscillator output
L1	P4	I/O	Programmable Digital I/O or Analog Input
L2	P5	I/O	Programmable Digital I/O or Analog Input and SOCOFF_WAKE
L3	P7	I/O	Programmable Digital I/O or Analog Input
L4	P9	I/O	Programmable Digital I/O or Analog Input
L5	VBAT	PWR	Battery supply
L6	LEXT1	A	Switcher Inductor
L7	LEXT2	A	Switcher Inductor
L8	VDDIOP	PWR	I/O power supply generated by PMU
L9	AVDD1P	PWR	Analog and RF core power supply generated by the PMU
L10	DVDD1P	PWR	Digital core power supply generated by PMU
L11	VBATLI	PWR	Lithium-ion battery input in place of VBAT, VBATLI must be connected to VBAT if not used

4 Mechanical Drawing

4.1 ATM3430e and ATM3430 7x7 mm, 56-pin QFN Package

Figure 4.1-1 ATM3430e and ATM3430 7x7 mm, 56-pin QFN Mechanical Drawing

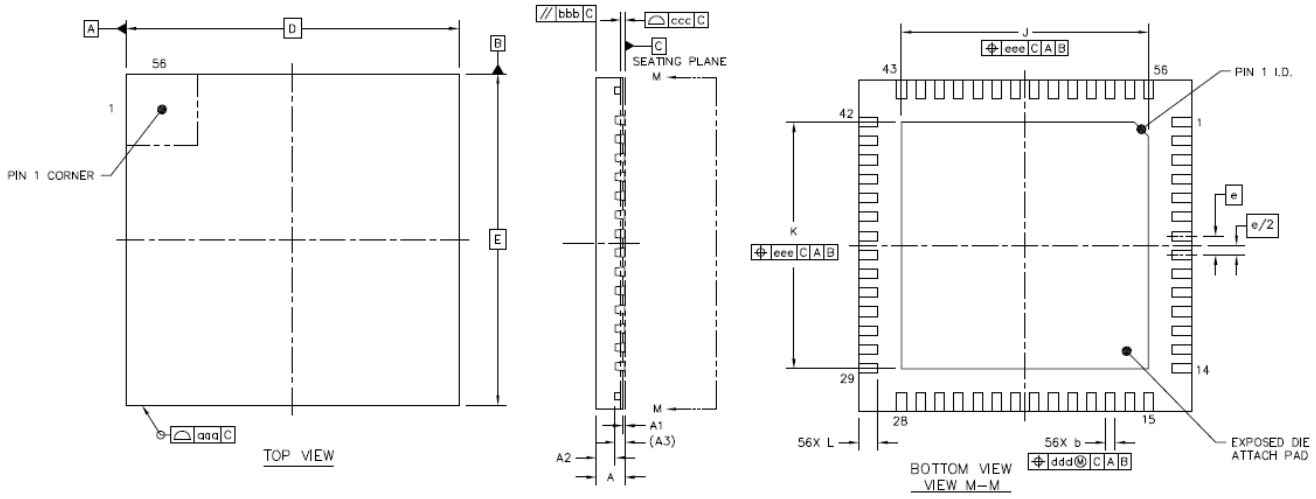


Table 4.1-1 ATM3430e and ATM3430 7x7 mm, 56-pin QFN Dimensions

		Symbol	Min	Nom	Max
Total Thickness		A	0.8	0.85	0.9
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	—	0.65	0.67
L/F Thickness		A3	0.203 REF		
Lead Width		b	0.15	0.2	0.25
Body Size	X	D	7 BSC		
	Y	E	7 BSC		
Lead Pitch		e	0.4 BSC		
EP Size	X	J	5.1	5.2	5.3
	Y	K	5.1	5.2	5.3
Lead Length		L	0.35	0.4	0.45
Package Edge Tolerance		aaa	0.1		
Mold Flatness		bbb	0.1		
Coplanarity		ccc	0.08		
Lead Offset		ddd	0.1		
Exposed Pad Offset		eee	0.1		

Notes:

1. All dimensions are in millimeters.
2. Coplanarity applies to leads, corner leads, and die-attached pads.

Figure 4.1-2 **ATM3430e and ATM3430 7x7 mm, 56-pin QFN Land Pattern**

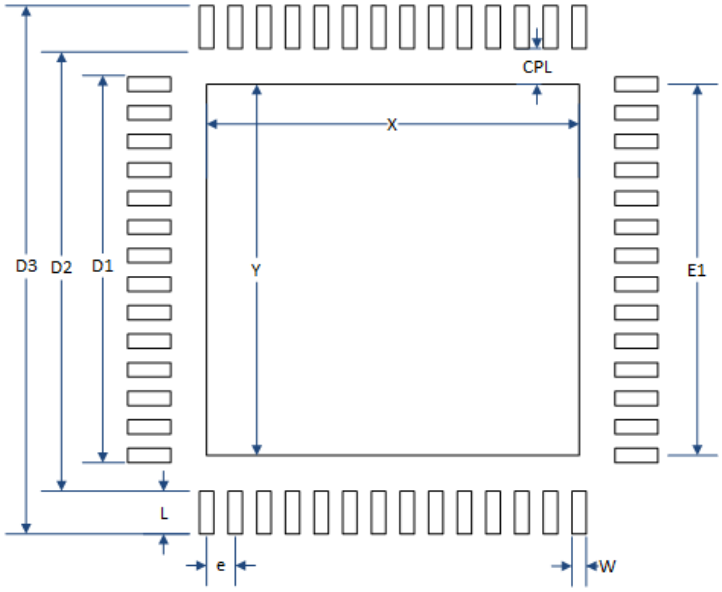


Table 4.1-2 **ATM3430e and ATM3430 7x7 mm, 56-pin QFN Land Pattern Dimensions**

Symbol	Typ
CPL	0.50
D1	5.4
D2	6.2
D3	7.4
e	0.4
E1	5.2
L	0.6
W	0.2
X	5.2
Y	5.2

Notes:

1. All dimensions are in millimeters (mm) unless otherwise noted.
2. The land pattern is based on the IPC-7351 guidelines. There may be other options specified in that publication.
3. The notes above and the land pattern are recommendations only. Customers may need to use different parameters as required for their application, materials, SMT process, and tooling requirements.

4.2 ATM3405 5x5 mm, 40-pin QFN Package - ATM3405-5PCAQK

Figure 4.2-1 ATM3405-5PCAQK 5x5 mm, 40-pin QFN Mechanical Drawing

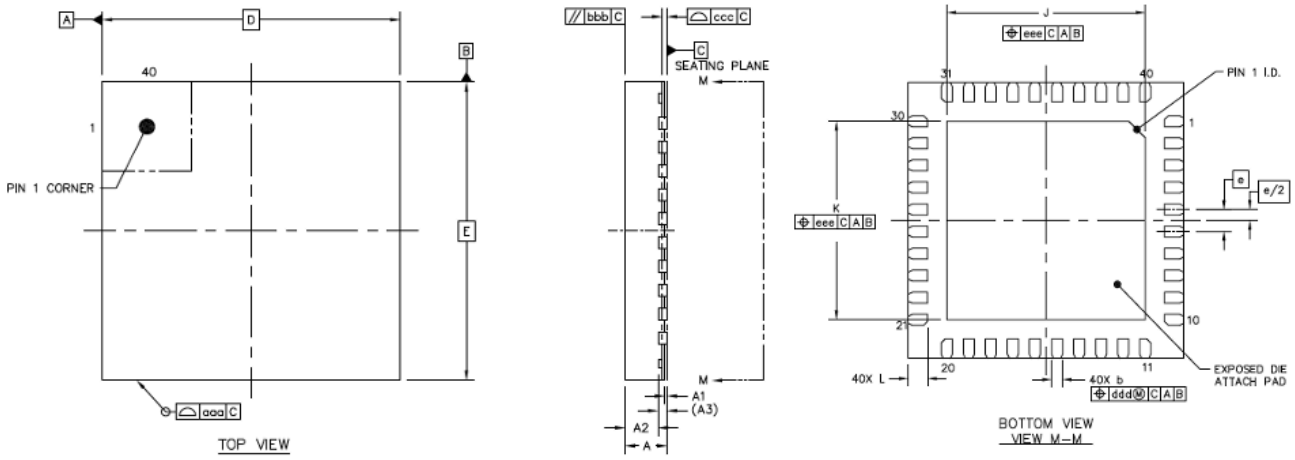


Table 4.2-1 ATM3405-5PCAQK 5x5 mm, 40-pin QFN Dimensions

		Symbol	Min	Nom	Max
Total Thickness		A	0.65	0.7	0.75
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	---	0.4	---
L/F Thickness		A3	0.152 REF		
Lead Width		b	0.15	0.2	0.25
Body Size	X	D	5 BSC		
	Y	E	5 BSC		
Lead Pitch		e	0.4 BSC		
EP Size	X	J	3.5	3.6	3.7
	Y	K	3.5	3.6	3.7
Lead Length		L	0.3	0.35	0.4
Package Edge Tolerance		aaa	0.1		
Mold Flatness		bbb	0.1		
Coplanarity		ccc	0.08		
Lead Offset		ddd	0.1		
Exposed Pad Offset		eee	0.1		

Notes:

1. All dimensions are in millimeters.
2. Coplanarity applies to leads, corner leads, and die-attached pads.

Figure 4.2-2 ATM3405-5PCAQK 5x5 mm, 40-pin QFN Landing Pattern

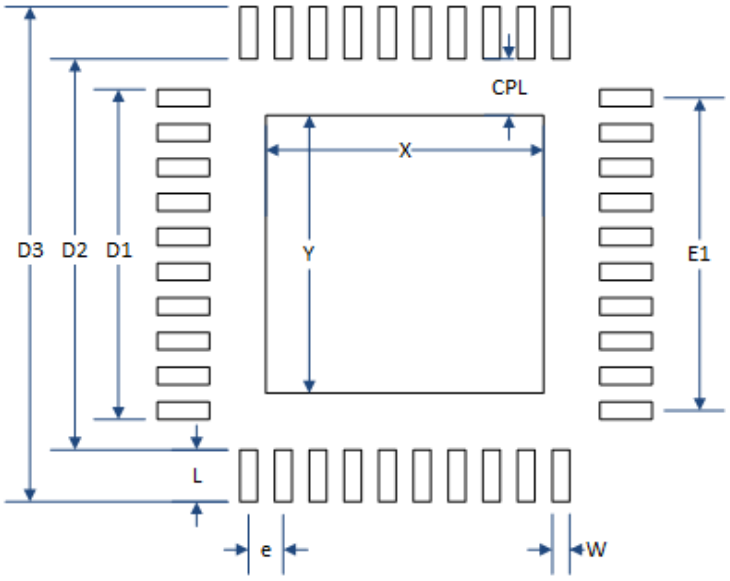


Table 4.2-2 ATM3405 5x5 mm, 40-pin QFN Land Pattern Dimensions

Symbol	Typ
CPL	0.65
D1	3.8
D2	4.5
D3	5.7
e	0.4
E1	3.6
L	0.6
W	0.2
X	3.2
Y	3.2

Notes:

1. All dimensions are in millimeters (mm) unless otherwise noted.
2. The land pattern is based on the IPC-7351 guidelines. There may be other options specified in that publication.
3. The notes above and the land pattern are recommendations only. Customers may need to use different parameters as required for their application, materials, SMT process, and tooling requirements.

4.3 ATM3405 5x5 mm, 40-pin QFN Package - ATM3405-5WCAQK

Figure 4.3-1 ATM3405-5WCAQK 5x5 mm, 40-pin QFN Mechanical Drawing

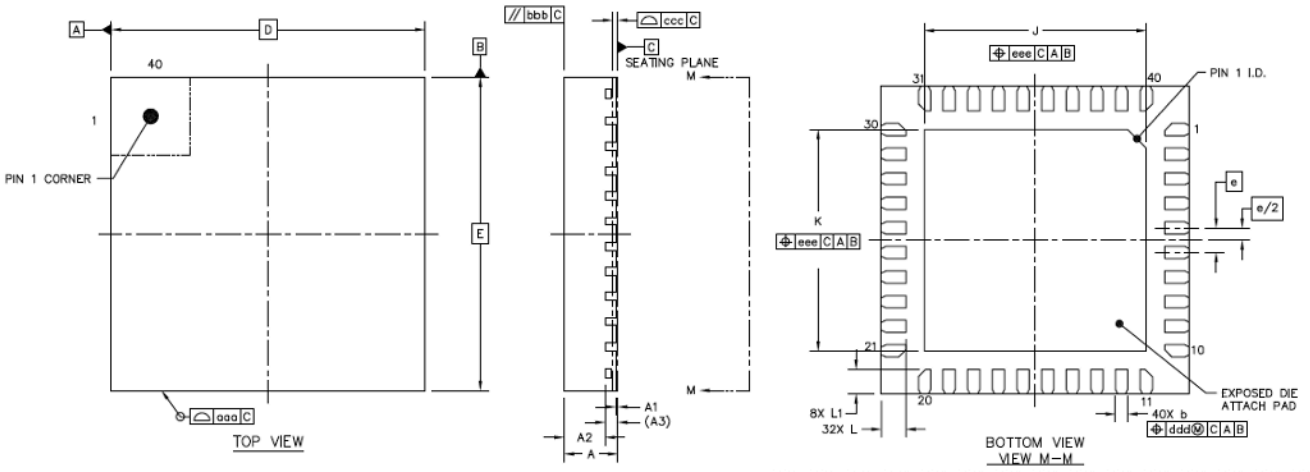


Table 4.3-1 ATM3405-5WCAQK 5x5 mm, 40-pin QFN Dimensions

		Symbol	Min	Nom	Max
Total Thickness		A	0.8	0.85	0.9
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	---	0.65	---
L/F Thickness		A3		0.203 REF	
Lead Width		b	0.15	0.2	0.25
Body Size	X	D		5 BSC	
	Y	E		5 BSC	
Lead Pitch		e		0.4 BSC	
EP Size	X	J	3.5	3.6	3.7
	Y	K	3.5	3.6	3.7
Lead Length		L	0.35	0.4	0.45
		L1	0.3	0.4	0.45
Package Edge Tolerance		aaa		0.1	
Mold Flatness		bbb		0.1	
Coplanarity		ccc		0.08	
Lead Offset		ddd		0.1	
Exposed Pad Offset		eee		0.1	

Notes:

1. All dimensions are in millimeters.
2. Coplanarity applies to leads, corner leads, and die-attached pads.

Figure 4.3-2 ATM3405-5WCAQK 5x5 mm, 40-pin QFN Landing Pattern

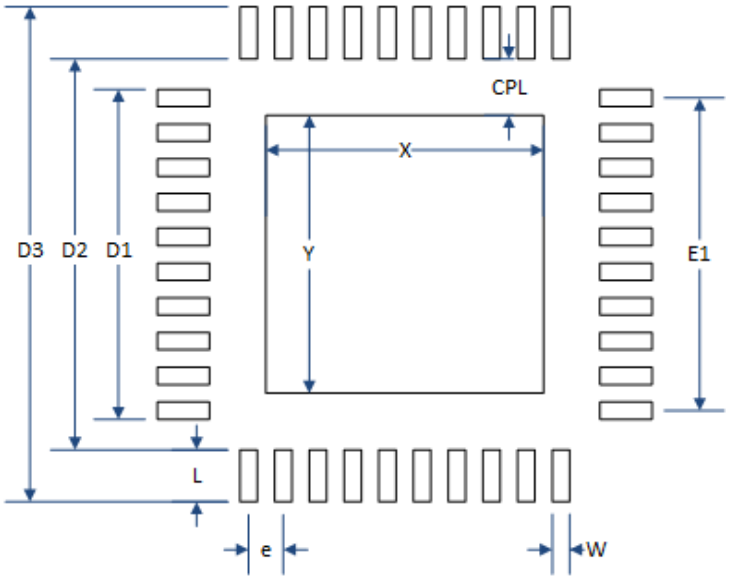


Table 4.3-2 ATM3405-5WCAQK 5x5 mm, 40-pin QFN Land Pattern Dimensions

Symbol	Typ
CPL	0.65
D1	3.8
D2	4.5
D3	5.7
e	0.4
E1	3.6
L	0.6
W	0.2
X	3.2
Y	3.2

Notes:

1. All dimensions are in millimeters (mm) unless otherwise noted.
2. The land pattern is based on the IPC-7351 guidelines. There may be other options specified in that publication.
3. The notes above and the land pattern are recommendations only. Customers may need to use different parameters as required for their application, materials, SMT process, and tooling requirements.

4.4 ATM3405 4x4 mm, 93-ball BGA Package

Figure 4.4-1 ATM3405 4x4 mm, 93-ball BGA Mechanical Drawing

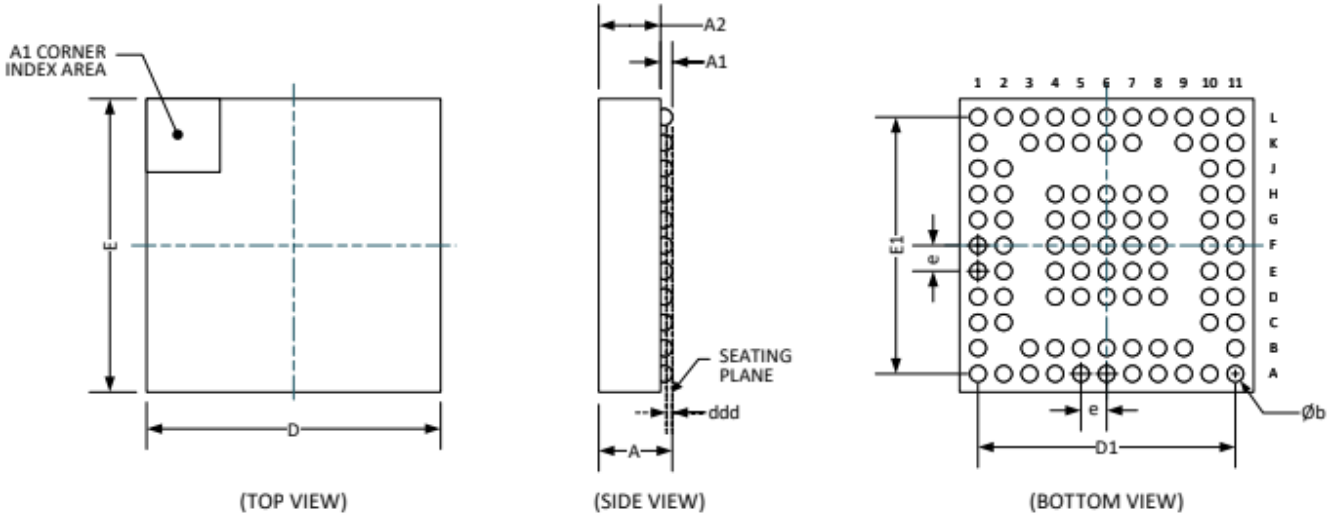


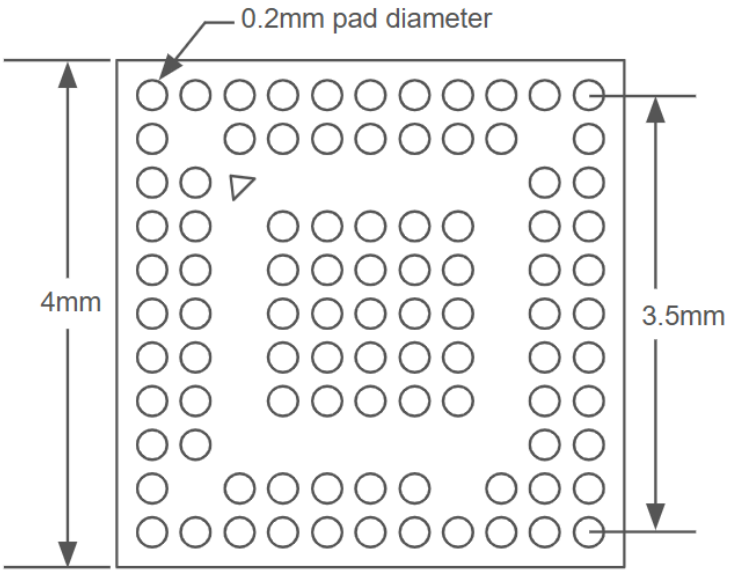
Table 4.4-1 ATM3405 4x4 mm, 93-ball BGA Dimensions

		Symbol	Min	Nom	Max
Total Thickness		A	0.835	0.91	1
Stand Off		A1	0.12	-	0.2
Package Thickness		A2		0.75 REF	
Body Size	X	D	3.9	4	4.1
	Y	E	3.9	4	4.1
Ball Pitch		e		0.35 BSC	
Ball Diameter		b	0.17	0.22	0.27
Edge Ball Center to Center	X	D1		3.5 BSC	
	Y	E1		3.5 BSC	
Coplanarity		ddd		0.08	

Notes:

1. All dimensions are in millimeters.
2. Coplanarity applies to leads, corner leads, and die-attached pads.
3. Soldering of 0.35mm ball pitch for the BGA package requires controlled reflow soldering processes. Utilization of the hand soldering process is not recommended. For optimal results, customers should consult their assembly partners.

Figure 4.4-2 ATM3405 4x4 mm, 93-ball BGA Landing Pattern (Top View)



Notes:

1. All dimensions are in millimeters (mm) unless otherwise noted.
2. The land pattern is based on the IPC-7351 guidelines. There may be other options specified in that publication.
3. The notes above and the land pattern are recommendations only. Customers may need to use different parameters as required for their application, materials, SMT process, and tooling requirements.

4.5 Solder Reflow Profile

The recommended reflow profile is per the IPC/JEDEC J-STD-020 specification for all the packages listed in the Mechanical Drawing. Please obtain the official specifications from JEDEC (https://www.jedec.org/).

4.6 Manual Soldering / Hot Soldering

Utilization of the manual soldering process is not recommended. For optimal results, customers should consult their assembly partners.

5 Part Ordering

Table 5-1 Part Ordering Numbers

Part Ordering Number	Product Line	Description	BLE	Energy Harvesting	GPIO	Maximum Number of General-Purpose Peripherals[5]						
						GADC (General single-ended channels listed)	UART	QSPI	SPI	I^2S	I^2C	PWM
ATM3405-5PCAQK-SR	ATM34 Bluetooth 6.0 Only Wireless MCU	ATM34 Series Bluetooth 6.0 Wireless MCU, **5x5 mm QFN 40 pin**, without energy-harvesting, **512KB NVM**, 256KB SRAM, Operating Temperature -40 °C to 85 °C, Small Reel, 7" 1K devices/reel	Y	N	21	5	2	1	2	1	2	8
ATM3405-5PCAQK	ATM34 Bluetooth 6.0 Only Wireless MCU	ATM34 Series Bluetooth 6.0 Wireless MCU, **5x5 mm QFN 40 pin**, without energy-harvesting, **512KB NVM**, 256KB SRAM, Operating Temperature -40 °C to 85 °C, sampling quantity in a tray, not for production volume	Y	N	21	5	2	1	2	1	2	8
ATM3405-5WCAQK-SR	ATM34 Bluetooth 6.0 Only Wireless MCU	ATM34 Series Bluetooth 6.0 Wireless MCU, **5x5 mm QFN 40 pin**, without energy-harvesting, **1536KB NVM**, 256KB SRAM, Operating Temperature -40 °C to 85 °C, Small Reel, 7" 1K devices/reel	Y	N	21	5	2	0	2	1	2	8

[5] Actual peripherals available depending on Pin Multiplexing configuration. Please refer to Pin Multiplexing for details.

Part Ordering Number	Product Line	Description			GPIO	Maximum Number of General-Purpose Peripherals[5]						
						GADC (General single-ended channels listed)	UART	QSPI	SPI	I^2S	I^2C	PWM
ATM3405-5WCAQK	ATM34 Bluetooth 6.0 Only Wireless MCU	ATM34 Series Bluetooth 6.0 Wireless MCU, **5x5 mm QFN 40 pin**, without energy-harvesting, **1536KB NVM**, 256KB SRAM, Operating Temperature -40 °C to 85 °C, sampling quantity in a tray, not for production volume	Y	N	21	5	2	0	2	1	2	8
ATM3405-5YCABV-UR	ATM34 Bluetooth 6.0 Only Wireless MCU	ATM34 Series Bluetooth 6.0 Wireless MCU, **4x4 mm BGA 93 ball,** without energy-harvesting, **2560KB NVM**, 256KB SRAM, Operating Temperature -40 °C to 85 °C, Small Reel, 7” 1K devices/reel	Y	N	46	7	3	0	2	1	2	8
ATM3405-5YCABV	ATM34 Bluetooth 6.0 Only Wireless MCU	ATM34 Series Bluetooth 6.0 Wireless MCU, **4x4 mm BGA 93 ball**, without energy-harvesting, **2560K NVM**, 256K SRAM, Operating Temperature -40 °C to 85 °C, sampling quantity in a tray, not for production volume	Y	N	46	7	3	0	2	1	2	8
ATM3430-5YCAQN-TR	ATM34 Bluetooth 6.0 Wireless MCU	ATM34 Series Bluetooth 6.0 Wireless MCU, **7x7 mm QFN 56 pin**, without energy-harvesting, 2560KB NVM, **256KB SRAM**, Operating Temperature -40 °C to 85 °C, Standard Reel, 13” 2.5K devices/reel	Y	N	31	7	2	0	2	1	2	8

Part Ordering Number	Product Line	Description			GPIO	Maximum Number of General-Purpose Peripherals[5]						
						GADC (General single-ended channels listed)	UART	QSPI	SPI	I^2S	I^2C	PWM
ATM3430-5YCAQN	ATM34 Bluetooth 6.0 Wireless MCU	ATM34 Series Bluetooth 6.04 Wireless MCU, **7x7 mm QFN 56 pin**, without energy-harvesting, 2560KB NVM, **256KB SRAM**, Operating Temperature -40 °C to 85 °C, sampling quantity in a tray, not for production volume	Y	N	31	7	2	0	2	1	2	8
ATM3430E-5YCAQN-TR	ATM34 Bluetooth 6.0 Wireless MCU	ATM34 Series Bluetooth 6.0 Wireless MCU, **7x7 mm QFN 56 pin**, **with energy-harvesting, 2560KB NVM,** 256KB SRAM, Operating Temperature -40 °C to 85 °C, Standard Reel, 13" 2.5K devices/reel	Y	Y	31	7	2	0	2	1	2	8
ATM3430E-5YCAQN	ATM34 Bluetooth 6.0 Wireless MCU	ATM34 Series Bluetooth 6.0 Wireless MCU, **7x7 mm QFN 56 pin, with energy-harvesting, 2560KB NVM,** 256KB SRAM, Operating Temperature -40 °C to 85 °C, sampling quantity in a tray, not for production volume	Y	Y	31	7	2	0	2	1	2	8

Reference Documents

Document Title	Description	Link
Arm® TrustZone Technology for the Armv8-M Architecture v2.1	TrustZone Architecture Manual	https://developer.arm.com/documentation
Arm® Cortex®-M33 Devices Generic User Guide Revision r1p0	Cortex M33 Users Guide	https://developer.arm.com/documentation
ARM®v8-M Architecture Reference Manual ARM DDI 0553A.e	ARMv8-M Core architecture reference	https://developer.arm.com/documentation

Revision History

Date	Version	Description
November 25, 2025	0.51	Updated Part Ordering Number (change ATM3405-5YCABV-SR to ATM3405-5YCABV-UR)
October 30, 2025	0.50	Updated Functional Block Diagram (remove R-cache); Updated SoC Power Consumption (4.2 V VBATLI); Updated Extended NVM Characteristics
September 30, 2025	0.49	Updated PMU Characteristics
September 23, 2025	0.48	Updated SoC Power Consumption (3 V VBAT)
September 16, 2025	0.47	Updated DVDD1P Output Voltage in PMU Characteristics
August 15, 2025	0.46	Added Table SoC Power Consumption (4.2 V VBATLI)
August 1, 2025	0.45	Updated Part Ordering. Added Operating Temperature info.
July 22, 2025	0.44	Updated contents to focus on main applications
July 1, 2025	0.43	Updated Maximum Electrical Ratings for VBATLI (Max), Updated Mechanical Drawing for ATM3405-5PCAQK and ATM3405-5WCAQK, Added ATM3405-5PCABV in Part Ordering
April 24, 2025	0.42	Updated Recommended Operating Conditions for VDDPA (Max)
April 14, 2025	0.41	Updated Recommended Operating Conditions for VBATLI (Max)
March 27, 2025	0.40	Added product ordering info for ATM3405 5x5 QFN with 1.5MB NVM
February 25, 2025	0.39	Updated Maximum VBAT in Maximum Electrical Rating, Maximum VBAT in Recommended Operation Conditions, Maximum TA in Recommended Operating Conditions, and ATM3405 4x4 mm, 93-ball BGA Dimensions
January 23, 2025	0.38	Updated ATM3405 4x4 mm, 93-ball BGA Mechanical Drawing
December 30, 2024	0.37	Added Maximum Number of General-Purpose Peripherals in Part Ordering Numbers

December 26, 2024	0.36	Added ATM3405 4x4 mm, 93-ball BGA Pinout, ATM3405 4x4 mm, 93-ball BGA Package, Peripherals and I/O
September 19, 2024	0.35	Updated Figure 3.1-1, Figure 3.2-1, Figure 3.3-1 (remove pin-1 bottom notch marking from package top-view)
July 24, 2024	0.34	Updated 1.1 MCU & Memory, 1.1.1Clocks (added RTC definition), 1.1.2 Reset, 1.1.3 Power Modes, Table 2-4 Radio Transceiver Characteristics, Table 2-7 Application ADC Characteristics, Table 2-9 SoC Power Consumption
June 20, 2024	0.33	Update to document title.
March 14, 2024	0.32	Update to Table 5-1 Part Ordering Numbers
February 16, 2024	0.31	Widespread electrical characteristic data updates. Updates to Section 1.1.1 Clocks, 1.4 Power Management Unit (PMU), 1.9 Peripherals and I/O. Updated Table 1.1-1 System Memory Map, Table 1.4-1 PMU External Pins, Table 2-2 WuRx Characteristics, Table 2-4 Radio Transceiver Characteristics, Table 2-5 PMU Characteristics#, Table 2-6 GPIO Characteristics, Table 2-7 Application ADC Characteristics, Table 2-8 Radio Power Consumption, Table 2-9 SoC Power Consumption, Table 2-11 NVM/RRAM Characteristics
December 22, 2023	0.30	Updates to formatting.
December 12, 2023	0.20	Updates to characteristics.
November 7, 2023	0.10	Initial release.

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