Connecting Atmosic SoC to Segger J-Link Adapters

User Guide

SUMMARY: The Segger J-Link interface is widely used in the industry for Flash programming. To reduce development time and costs, Atmosic Technologies offers software compatible with Segger J-Link adapters.

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Connecting Atmosic SoC to Segger J-Link Adapters User Guide
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Acronyms and Abbreviations

Acronyms	Definition
EVK	Evaluation Kit
EVB	Evaluation Board

1. Overview

The Segger J-Link interface is widely used in the industry for Flash programming. To reduce development time and costs, Atmosic Technologies offers software compatible with Segger J-Link adapters.

This user guide provides instructions on:

- Connecting Atmosic's Serial Wire Debug (SWD) signals to Segger J-Link adapters
- Implementing a setup using Atmosic EVKs and Segger J-Link adapters
- Programming Atmosic ATM2/3, ATM33, and ATM34 solutions using J-Flash software
- Programming Atmosic ATM2/3, ATM33, and ATM34 solutions with the Atmosic Flash Programming Tool via the Segger J-Link adapters

2. Hardware Connections

2.1 Connection Requirements

For all the Atmosic solutions, the signals in Table 1 are needed to Flash the code.

Sequence	Signal Name	Functions
1	VBAT/VBATLI	Power the Wireless SoC
2	VDDIO	Set the IO Reference Voltage Level
3	BBOOT	Benign Boot Mode Selection (Input)
4	PWD	Power Down Reset (Input)
5	SWDIO	SWD Data Read/Write
6	SWDCLK	SWD Clock
7	GND	Ground

Table 1 - Connection Requirements

Figure 1 illustrates the signal sequences.

1. **Powering the Chip** – The first step is to power the chip and set the reference voltage level, enabling communication with interface solutions like Segger J-Link, which is used in this document.
2. **Selecting the Boot Mode** – The J-Link adapter sets the BBOOT signal high. Since the CPU checks the boot mode only during a cold boot, the PWD reset is toggled to force the CPU into a cold boot. The cold boot process begins when PWD is released.
3. **Benign Boot Mode** – When the BBOOT pin is set high during a cold boot, the system enters benign boot mode. This mode ensures that no other CPU activities interfere with the process, preventing conflicts. It is particularly useful for R&D and retry operations in production lines.

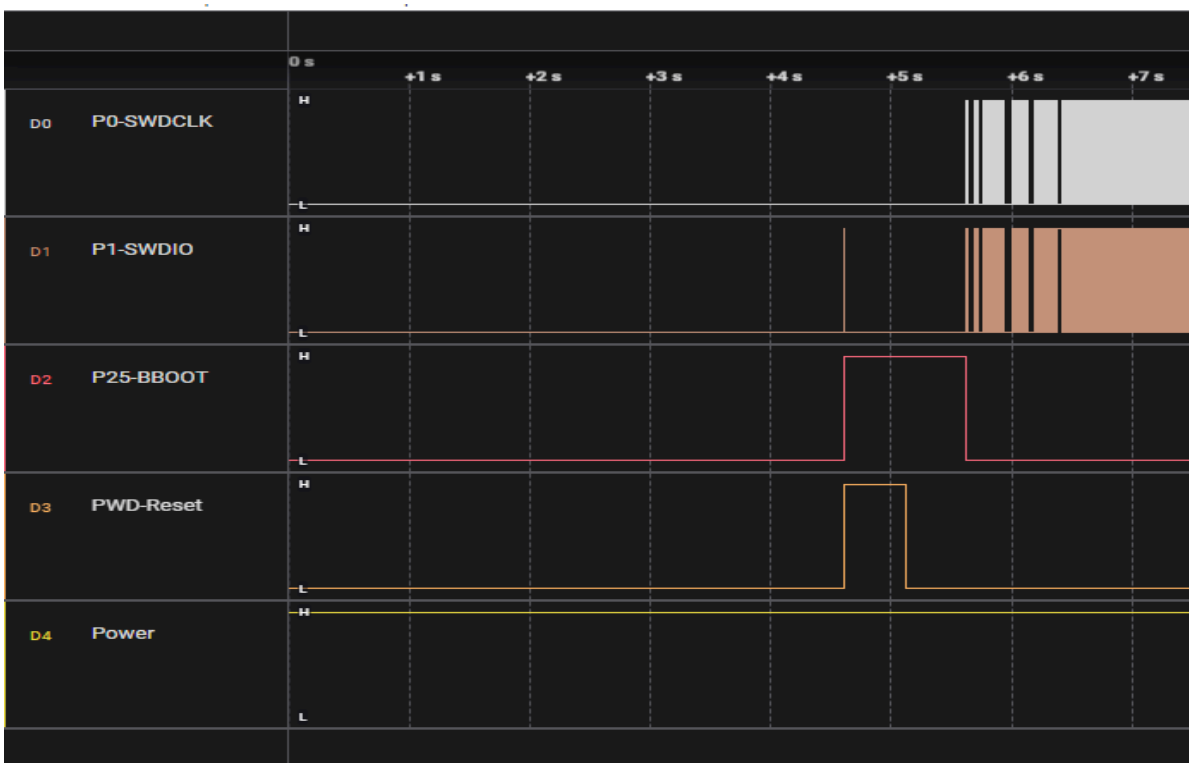


Figure 1 - Programming Signal Sequence: Power (VBAT/VDDIO)→BBOOT→PWD→ SWD

2.2 Atmosic and Segger J-Link Connections

Atmosic solutions need PWD and BBOOT signals from the Segger J-Link adapter to select boot mode. The signals are not in the standard J-Link interface. The unused pins, 5 and 11, are used to generate the PWD and BBOOT signals, see Figure 2 for the Segger J-Link Pinout.

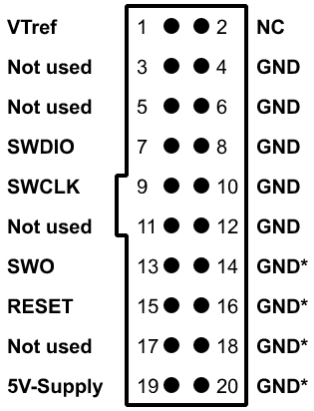


Figure 2 - Segger J-Link SWD Interface Pinout

The only power output from the Segger J-Link interface is 5V-supply at pin 19. For programming purposes, it is highly recommended to use a voltage between 3.2V and 2.9V at VBAT or VBATLI pins. See Figure 3 for the connection block diagram.

NOTE: Do not connect any 5 V supply directly to the Atmosic SoC's VBAT/VBATLI pins.

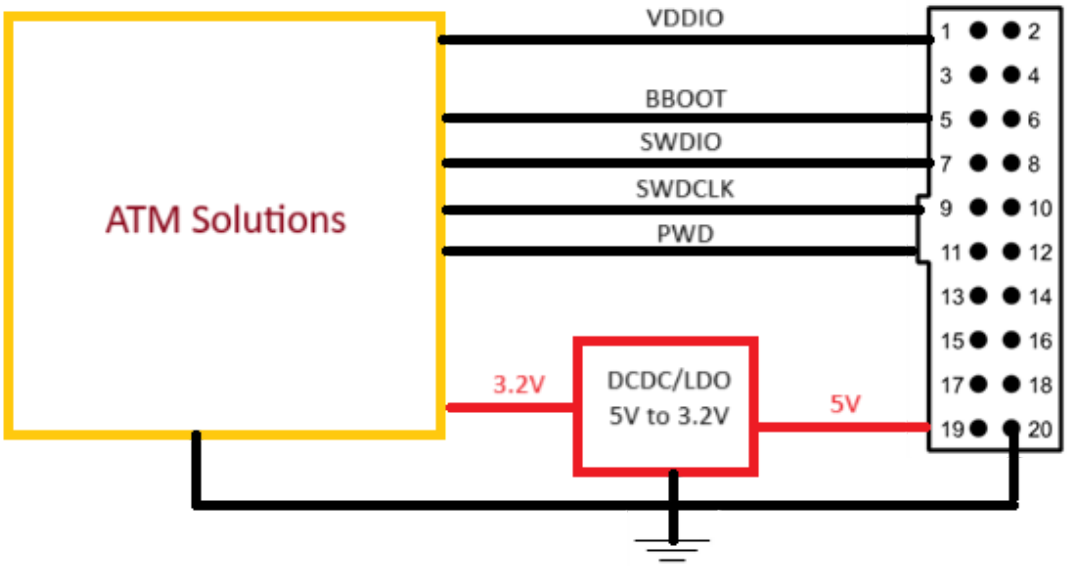


Figure 3 - Block Diagram of ATM Solutions - Segger J-Link Connection

As shown in Figure 3, users need to add a DCDC or LDO to convert 5 V to 3.2 V to feed the power to the ATM chipsets. Users can also use a bench supply, or any stable voltage source to generate 3.2 V to power up the SoC as long as the source can output enough power, e.g. 400mA for the whole programming process. The power requirement may vary depending on the peripheral circuits, and memory of the products.

Below is an example of building the connections between an ATM solution and a Segger J-Link adapter.

1. Find the test points or the signal traces of the signals listed in Table 1 from the design schematic and locate the test points on the PCB (e.g. Figure 4).

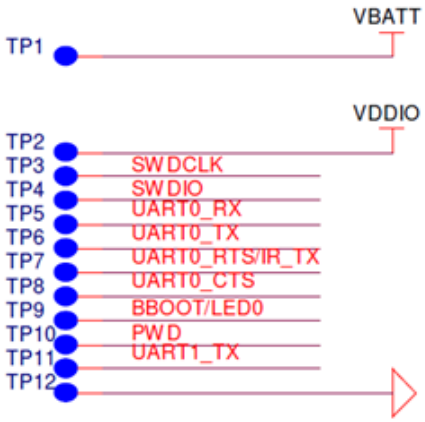


Figure 4 - Test Points on the ATM solution side

2. Connect VBAT (TP1) in Figure 4 to 3.2 V supply.
3. Connect the ground (TP12) to the supply ground with the J-Link ground (pin20) as shown in Figure 3.
4. Connect TP2 VDDIO to J-Link pin1 VTref.
5. Connect TP3 SWDCLK to J-Link pin9.
6. Connect TP4 SWDIO to J-Link pin7.
7. Connect TP9 BBOOT to J-Link pin5.
8. Connect TP10 PWD to J-Link pin11.

3. Proof of Concept with Atmosic EVBs

3.1 ATM2/3 EVB to Segger J-Link Connection Guide

ATM2/3 EVBs feature the J3 connector (Figure 5), allowing users to directly connect signals to the Segger J-Link adapter using jumper wires (Figure 6). For proof of concept (PoC), the VBAT pin of the ATM2/3 can be connected to a 3 V bench power supply.

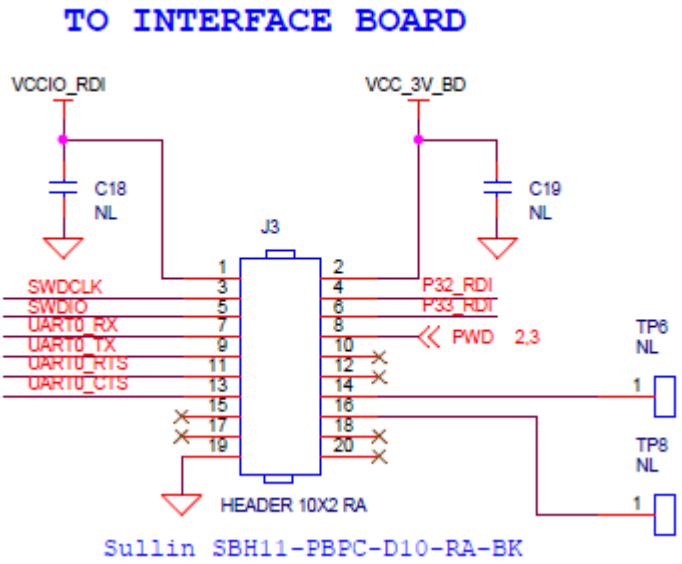


Figure 5 - Connection Interface of the ATM2/3 EVB

Figure 6 - Female-to-Female Jumper Wires

Follow Table 2 to build the test setup.

Signal Name	ATM2/3	J3 20-Pin connector	Segger J-Link
VCC_3V_BD	3V Bench Supply	Pin2 (VCC_3V_BD)	N/A
VCCIO (VDDIO)	VDDIO	Pin1 (VCCIO_RDI)	Pin1 (VTref)
BBOOT	P32	Pin4 (P32_RDI)	Pin5
PWD	PWD	Pin8 (PWD)	Pin11
SWDCLK	P1	Pin3 (SWDCLK)	Pin9 (SWDCLK)
SWDIO	P2	Pin5 (SWDIO)	Pin7 (SWDIO)
GND	GND	Pin19 (GND)	Pin20 (GND)
Additional EVB Board Configurations			
VBAT - VCC_3V_BD	Install JP7	N/A	N/A
VDDIOP-VCCIO	Installed J1 Pin1-2&3-4	N/A	N/A
VCCIO-VDDIO	Install JP5	N/A	N/A

Table 2 - ATM2/3 to Segger J-Link Connections

Since the Segger J-Link adapter might not highlight the pin orientation, the pin orientation can be found by checking the continuity between pin 18 and pin 20. See Figure 7. The pins 1/3, 2/4, and 17/19 will show open in the continuity tests. To save time, if users use Segger J-link Plus Compact, they can find the pin orientation from Figure 7.

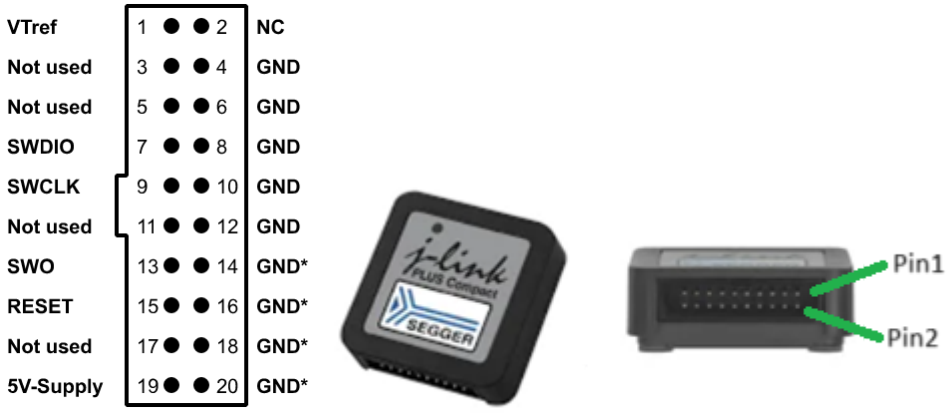


Figure 7 - Segger J-Link Plus Compact Pin Orientations

3.2 ATM33/34 EVB to Segger J-Link Connection Guide

ATM33 and ATM34 EVBs have the Segger J-Link chipset (MK22) mounted on the EVBs. To connect the ATM33/ATM34 to the external Segger J-Link adapter, the on-board J-Link chipset MK22, see Figure 8, must be disconnected and isolated from the connection between ATM33/34 and the external J-Link adapter.

Figure 8 - On-Board J-Link MK22

The MK22 digital connections can be isolated by inserting a jumper on the JP11 header, See Figure 9. The analog switches that isolate the MK22 from the ATM33 or ATM34 will be powered up through the J-Link Adapter. This is to prevent high leakage current leaking from J-Link Adapter to MK22 IO pins.

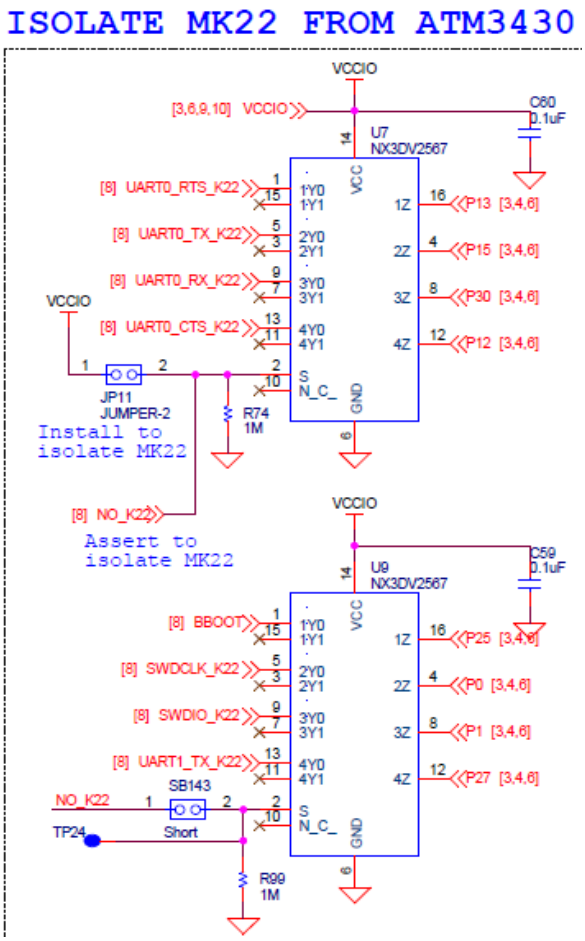


Figure 9 - Analog Switches on the EVBs to Isolate the Digital Connections

The connections between the external Segger J-Link Adapter and ATM33/34 EVBs can be wired through the J12 50-pin connector I/O interface, Figure 10, on the EVB. To program the Flash, the signals needed are VBAT, VDDIO, SWDCLK, SWDIO, PWD, and BBOOT. As shown in Figure 9, the SWDCLK is assigned to P0, SWDIO is assigned to P1, and BBOOT is assigned to P25. Users can follow Table 3 to connect the ATM33/34 EVB with the external Segger J-Link Adapter with female-to-female jumper cables. Since the 50-pin connector I/O interface pin assignments might be different in different EVB designs. Please refer to the signal names and connect the EVBs to the Segger J-Link accordingly.

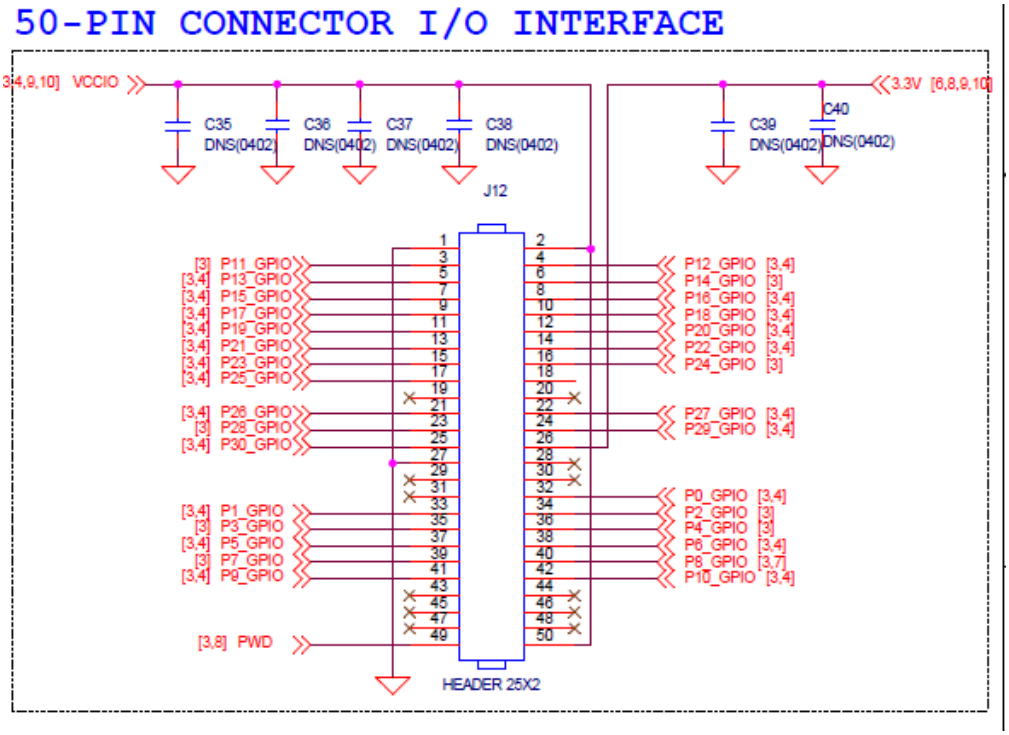


Figure 10 - 50 Pin Header Connector on ATM33/34 EVB

Signal Name	ATM33/ATM34	J12 50-Pin connector	Segger J-Link
VBAT/VBATLI	Power from USB port	NC	N/A
VDDIO	VDDIO	Pin2 (VCCIO)	Pin1 (VTref)
BBOOT	P25	Pin17 (P25_GPIO)	Pin5
PWD	PWD	Pin49 (PWD)	Pin11
SWDCLK	P0	Pin32 (P0_GPIO)	Pin9 (SWDCLK)
SWDIO	P1	Pin33 (P1_GPIO)	Pin7 (SWDIO)
GND	GND	Pin1 (GND)	Pin20 (GND)
VBUS	TP21	N/A	Pin19 (5V supply)
Additional EVB Board Configurations			
VDDIOP	Installed J23 Pin2-3	N/A	N/A
Analog Switch	Installed JP11	N/A	N/A
VBAT	Install J21 Pin1-2	N/A	N/A

Table 3 - ATM33/34 EVB to Segger J-Link Connections

4. Programming ATM2/3, ATM33/34 with Segger Tools

4.1 Segger J-Link Adapter Configuration

To enable the Segger J-Link adapter's 5 V power supply, follow the configuration steps outlined below. This 5 V supply powers the EVB, so ensure the USB cable is not connected to the EVB. Note that this step is mandatory for ATM33/34 EVBs but optional for ATM2/3.

The J-Flash Lite is the free programming tool offered by Segger. The tool can be downloaded at https://www.segger.com/downloads/jlink/.
After the tool is installed, connect the J-Link adapter to the PC with the USB port and open the J-Link Commander in the Windows start menu → all apps → Segger - J-Link version as shown in Figure-11.

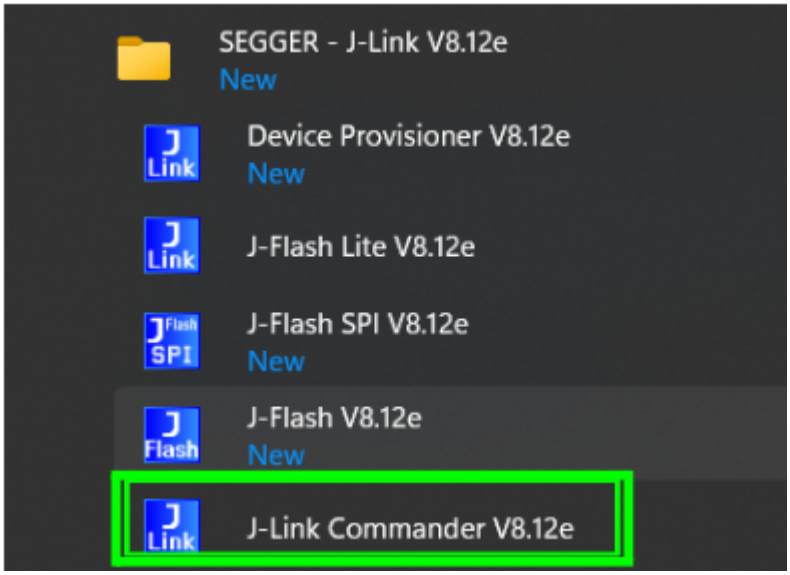


Figure 11 - J-Link Commander

Issue the command "power on perm" see Figure-12. This command will turn on the 5 V supply from the J-Link Adapter. The voltage can be measured from pin 19. The 5 V can be used for the ATM33/34 PoC because the ATM33/34 EVBs have the LDO to convert 5 V to 3 V, see Table 3 VBUS connection. For ATM2/3 PoC, a 5 V supply is not used and the EVBs can only be powered up by a 3 V bench supply because there is no LDO on board like the ATM33/34 EVBs can be used to generate 3V.

```
Type "connect" to establish a target connection, '?' for help
J-Link>power on perm
J-Link>
```

Figure 12 - J-Link Command to Turn On the 5 V Supply

4.2 Segger J-Flash Lite

At this point, the hardware connection should be ready, see section 3.1 for ATM2/3 and section 3.2 for ATM33/34. Users are expected to have the software binaries precompiled, as this document does not cover the code compilation process. For a base example, to program the SoC, three binary files are required: application .bin, NVDS .bin, and bootloader/MCUboot .bin. Users can also refer to the Atmosic SDK User Guide to learn how to compile the binary images. In this guide, the BLE_ADV example is used. The application .bin file for the BLE_ADV example is called BLE_adv.bin. The NVDS .bin file is called flash_nvds.bin. Both files can be found under the BLE_adv folder after the code is compiled. The bootloader file is called bootloader.bin and can be found under the bootloader folder, See Figure 13.

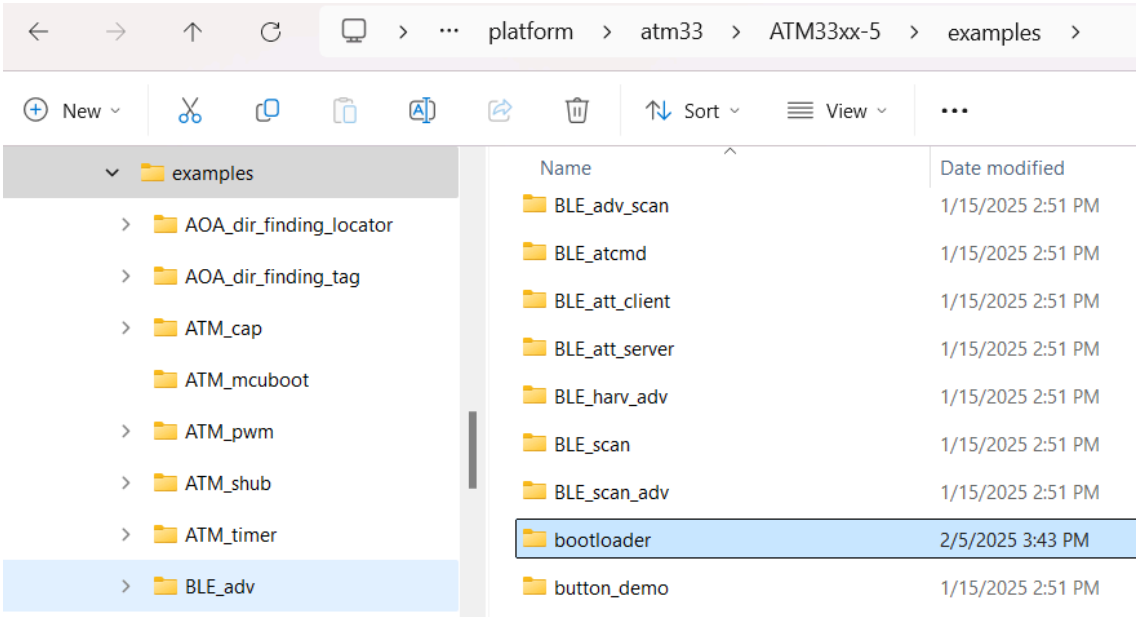


Figure 13 - File Locations

To program ATM2/3, please follow the following steps:

1. Turn on the 3 V bench supply to power up the chip
2. Connect the J-Link adapter to the PC

To program ATM33/34

1. Connect the J-Link adapter to the PC

The rest of the procedures are the same among ATM2/3 and ATM33/34. ATM3325 is used as an example.

1. Open the J-Flash Lite, Figure 14

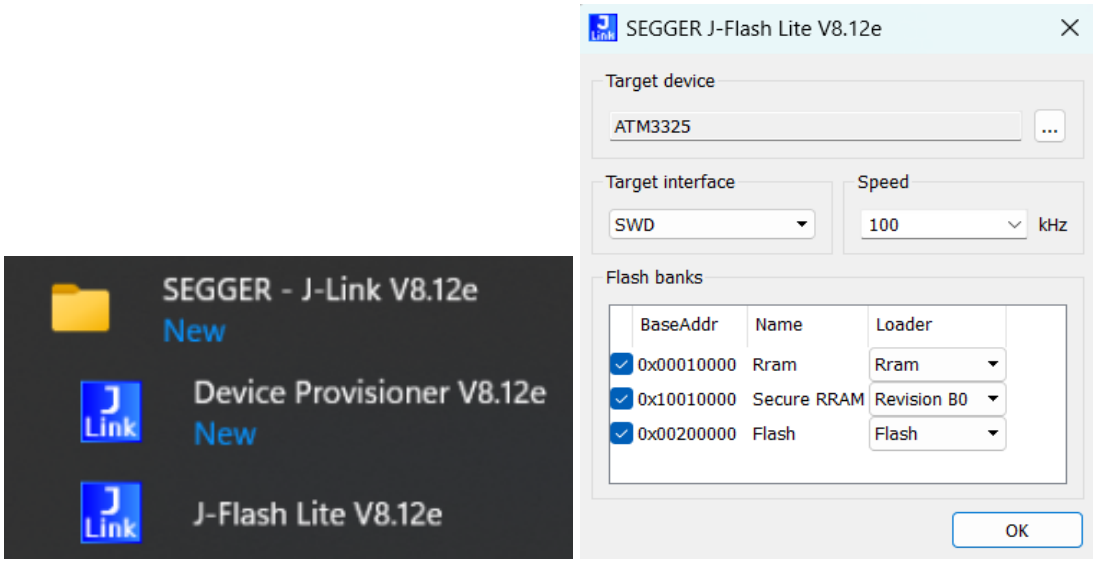
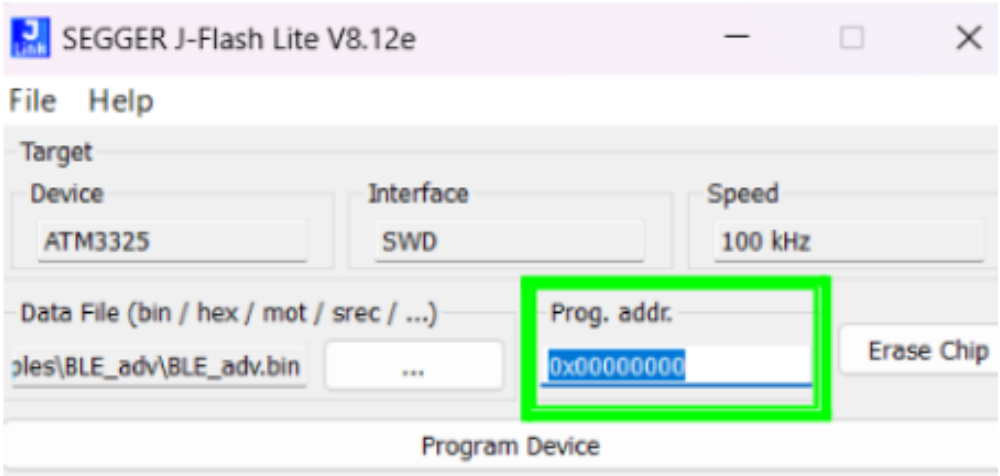
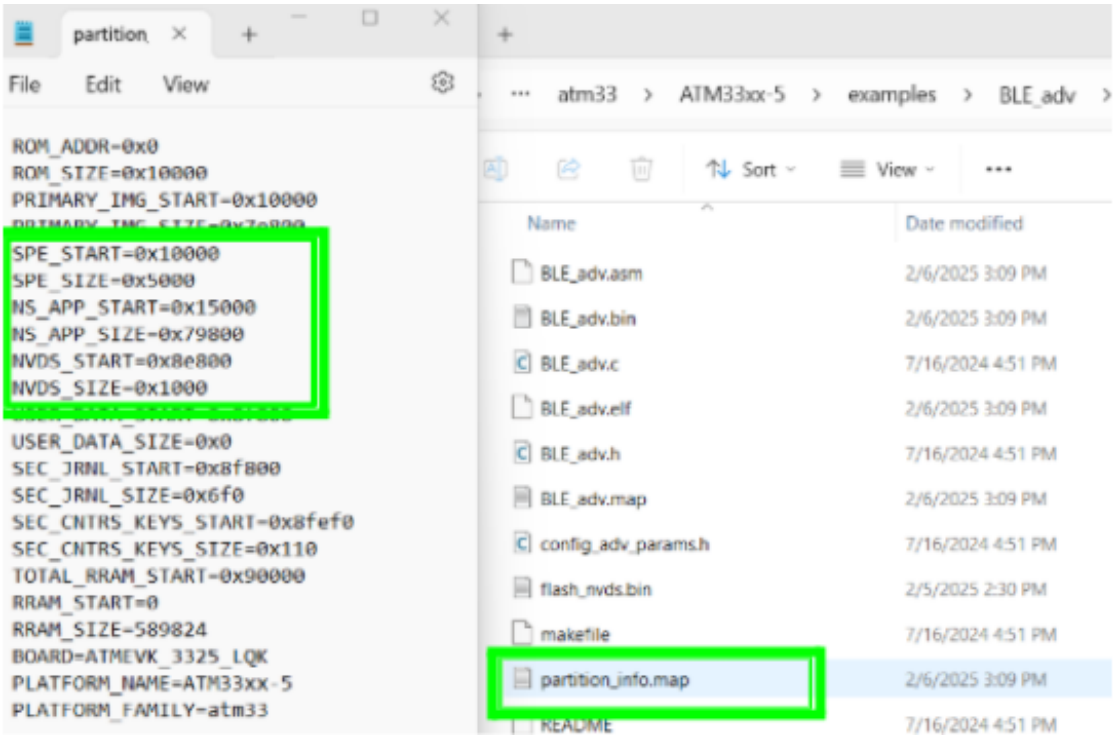


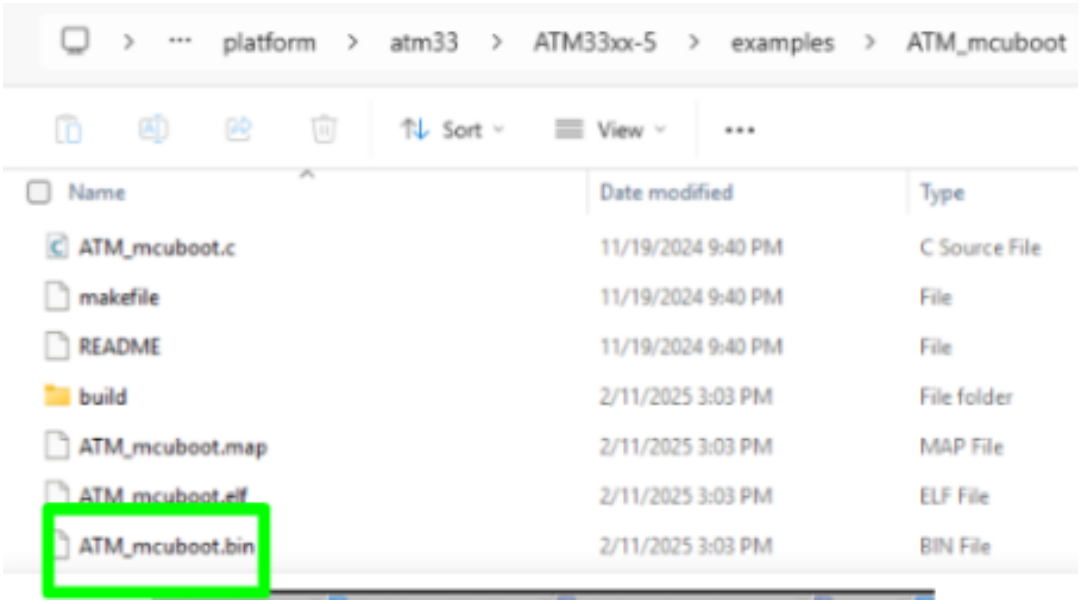
Figure 14 - J-Flash Lite

2. Select the target device and 100KHz, the ATM3325 is selected as an example, see Figure 14. Click OK.
3. Select the binary file, this process will be repeated three times for the three different binary files. The sequence doesn't matter.
4. Once the file is selected, the `Prog. addr.` box will be added to the GUI. The `Prog. addr.` is the partition starting address. The information can be found in the partition_info.map file. The default build partition map start address for the ATM33 SoC is NS_APP_START=0x15000 (BLE_adv.bin). The start address of the bootloader.bin location is SPE_START=0x10000. The start address for the flash_nvds.bin is NVDS_START=0x8e800. Reminder to review partition_info.map for precise address



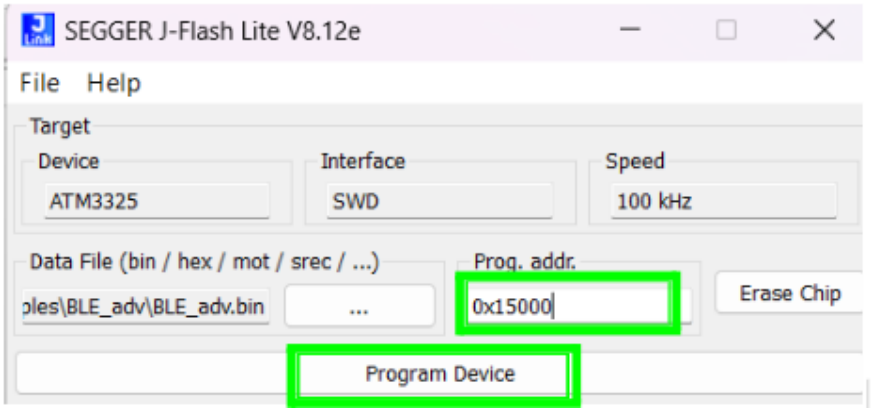


If the MCUboot is used, the mcuboot address information can also be found in the partition_info.map. The MCUboot.bin file can be found under the ATM_mcuboot folder.



```
ROM_ADDR=0x0
MCUBOOT_START=0x10000
MCUBOOT_SIZE=0xc000
APP_START=0x1c000
APP_SIZE=0x72000
NVDS_START=0x8e800
NVDS_SIZE=0x1000
USER_DATA_SIZE=0x0
SEC_JRNL_START=0x8f800
SEC_JRNL_SIZE=0x6f0
SEC_CNTRS_KEYS_START=0x8fef0
SEC_CNTRS_KEYS_SIZE=0x110
SECONDARY_SLOT_TRAILER_START=0x75000
SECONDARY_SLOT_TRAILER_SIZE=0x1000
MCUBOOT_MAX_IMG_SECTORS=114
TOTAL_RRAM_START=0x90000
EXT_FLASH_START=0x200000
EXT_FLASH_SIZE=0x80000
EXT_FLASH_MCUBOOT_SCRATCH_START=0x200000
EXT_FLASH_MCUBOOT_SCRATCH_SIZE=0x4000
EXT_FLASH_OTA_STAGING_START=0x204000
EXT_FLASH_OTA_STAGING_SIZE=0x72000
```

5. In this example, enter 0x15000 for the BLE_adv.bin file and click the Program Device button.



6. After BLE.adv.bin is loaded, select flash_nvds.bin, and enter 0x8e800 into the `Prog. addr.` box and click program device
7. Then, select bootloader.bin (this file is under the bootloader folder), enter 0x10000 to the `prog. addr.` Box. and click the Program Device button.

The J-Flash Lite tool must load three files to complete the programming process. Alternatively, Atmosic provides a Flash Programming Tool that simplifies the process, provided the hardware setup remains the same as described in Chapters 2 and 3. The tool can be found in the Atmosic customer portal below.

https://atmosic.com/portal/development-tools/

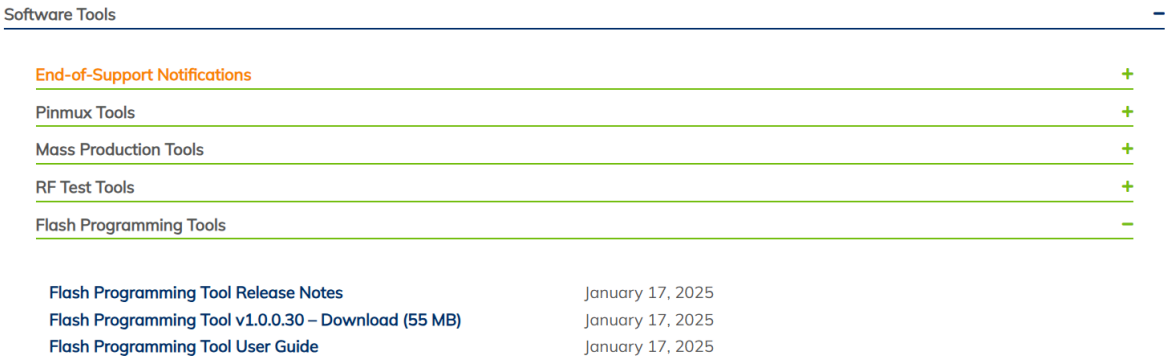


Figure 15 - Atmosic Flash Program Tool Download Page

The Atmosic Flash Programming Tool uses the .atm file archive format. After the code is compiled, the app .bin/elf file, e.g. BLE_adv.bin, flash_nvds.bin, and bootloader.bin file can be merged to one .atm file by the “make build_archive” command. The detailed information can be found in the Atmosic SDK User Guide.

4.3 Validation with UART1 Debug Port

To validate if the code is loaded successfully to the memory, users can use the UART1 debug port to print the debug messages. To read the console debug messages, simply remove the connections with the Segger-Jlink adapter. ATM2/3 EVKs need to disconnect the external bench supply and connect the board with the Atmosic interface board. The details of how to set up the debug console can be found in the Atmosic SDK User Guide section 3.4 for setting up the debug interface. The file can be found in the Atmosic customer portal https://atmosic.com/portal/welcome/ and enter the document name to find the document file.

ATM33/34 EVKs need to remove the jumper JP11 in addition to removing the Jlink connections and plug in the USB cable. The details of how to set up the debug interface can be found also in the Atmosic SDK User Guide section 3.4.

5. Troubleshooting

- Make sure the cables/wiring is to a minimal length when connecting the DUT to the J-Link adapter
- Programming fails inconsistently. Try lowering the CLK speed

Reference Documents

Title	Document Number
ATM33/e Series Evaluation Kit User Guide	ATM33_e-UGEVK
ATM34/e Series Evaluation Kit User Guide	6441-xxxx-xxxx
SDK User Guide	6844-xxxx-xxxx
ATM2/ATM3 Evaluation Kit User Guide	ATM2_ATM3-UGEVK

Revision History

Date	Version	Description
February 26, 2025	0.50	Initial version created

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