

ATM3405 BGA Eval Board (JLink OB)

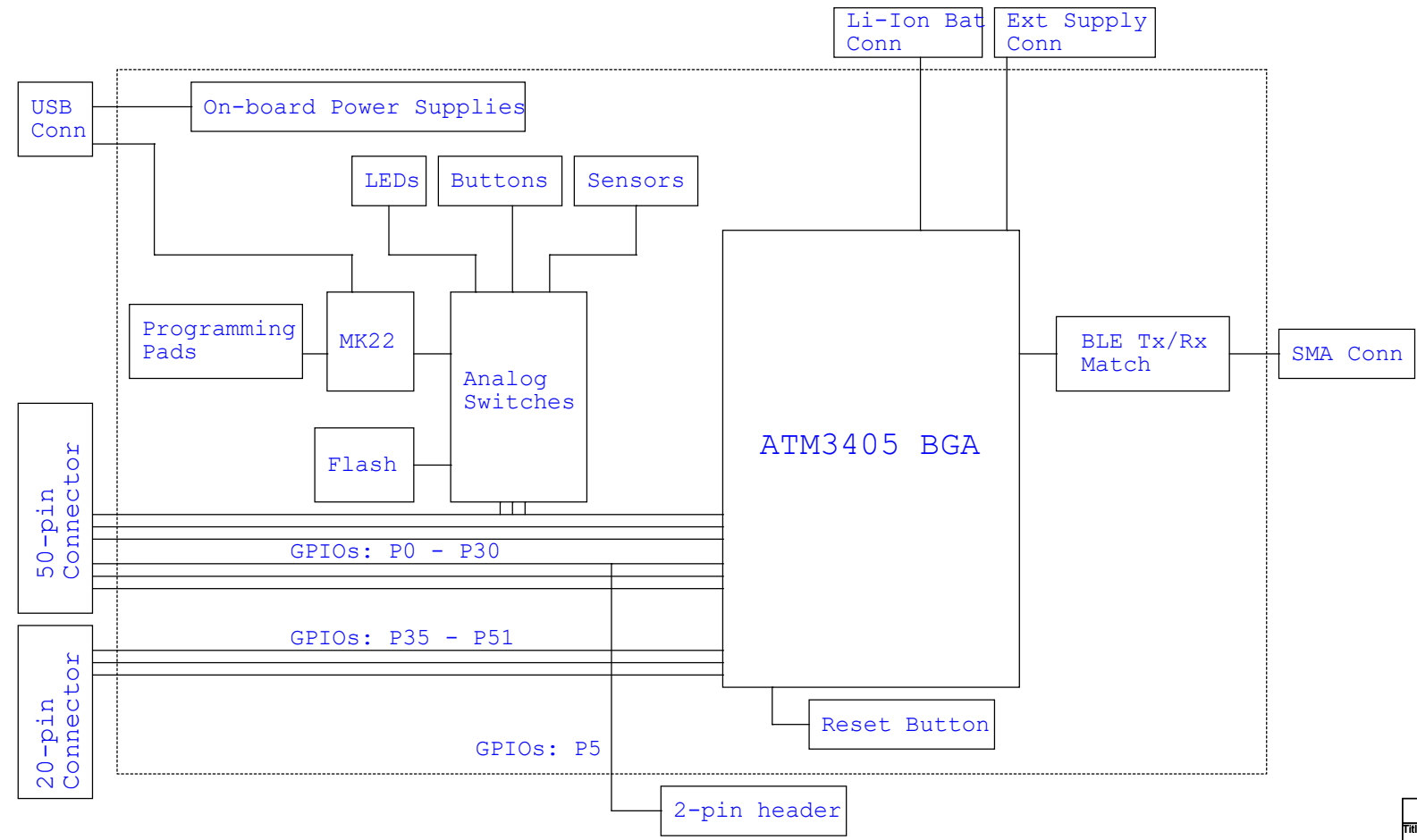
| Release Date | Revision | Design Eng. | Design Notes |
|--------------|----------|---------------|---|
| 11/04/24 | -00 | Chris Tsailin | Initial release, based on the latest Perth 3430e EVB, with VDDIO-VCCIO tracking circuit added |
| 3/18/25 | -01 | Andy Dao | L14 changed to 3.3nH; C2, C8 changed to DNS, C68 to 1uF; Channel Sounding: C11=4.7uF, C13=10uF; |
| 6/27/25 | -02 | Joe Chen | 1. C6 changed from 1.0uF(0402) to 4.7uF(0402) 2. C11 changed from 4.7uF(0402) to 1.0uF(0402) 3. C68 changed from 1uF(0402) to 0ohm(0402) |
| 12/17/25 | -04 | Andy Dao | 1. C5 changed from 4.7uF(0402) to 10uF(0402) 2. C6 changed from 4.7uF(0402) to 10uF(0402) 3. Correct pin names F10 and G10 of U1 to NC (traces to these pins will be removed in next pcb rev) |

Atmosic Technologies Proprietary and Confidential

Atmosic Technologies, Inc
2130 Gold Street, Suite 200
San Jose, CA 95002

| | | |
|---|------------------------------------|------------|
| ATMOSIC TECHNOLOGIES INC | | |
| Title ATM3405 BGA Eval Board (JLink OB) - Revision notes | | |
| Size B | Document Number 101-04-510-xxxx | Rev 0.2 |
| Date: Wednesday, December 17, 2025 Sheet 1 of 8 | | |

Block Diagram



| ATMOSIC TECHNOLOGIES INC | | |
|---|------------------------------|--------------|
| Title | | |
| ATM3405 BGA Eval Board (JLink OB) - Block diagram | | |
| Size | Document Number | Rev |
| B | 101-04-510-xxxx | 0.2 |
| Date: | Wednesday, December 17, 2025 | Sheet 2 of 8 |

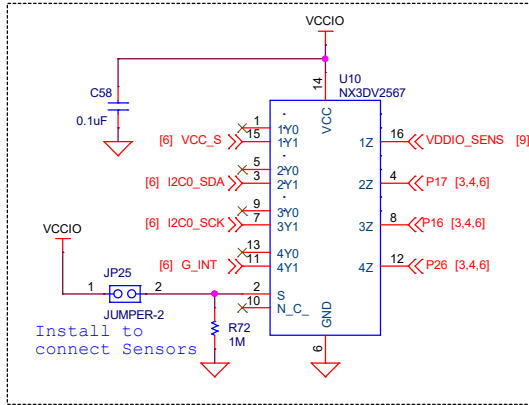
GPIO MUX

[3,6] P0_GPIO >> <<P0 [3,4,6]
 [3,6] P1_GPIO >> <<P1 [3,4,6]
 [3,6] P2_GPIO >> <<P2 [3,6]
 [3,6] P3_GPIO >> <<P3 [3,6]
 [3,6] P4_GPIO >> <<P4 [3,6]
 [3,6] P5_GPIO >> <<P5 [3,4,6]
 [3,6] P6_GPIO >> <<P6 [3,4,6]
 [3,6] P7_GPIO >> <<P7 [3,6]
 [3,6,7] P8_GPIO >> <<P8 [3,6,7]
 [3,6] P9_GPIO >> <<P9 [3,4,6]
 [3,6] P10_GPIO >> <<P10 [3,4,6]
 [3,6] P11_GPIO >> <<P11 [3,6]
 [3,6] P12_GPIO >> <<P12 [3,4,6]
 [3,6] P13_GPIO >> <<P13 [3,4,6]
 [3,6] P14_GPIO >> <<P14 [3,6]

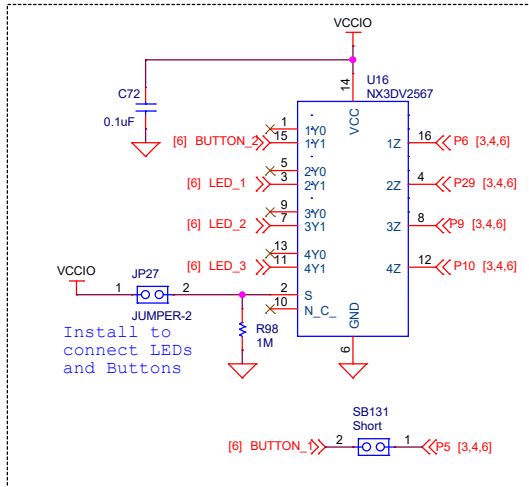
[3,6] P15_GPIO >> <<P15 [3,4,6]
 [3,6] P16_GPIO >> <<P16 [3,4,6]
 [3,6] P17_GPIO >> <<P17 [3,4,6]
 [3,6] P18_GPIO >> <<P18 [3,4,6]
 [3,6] P19_GPIO >> <<P19 [3,4,6]
 [3,6] P20_GPIO >> <<P20 [3,4,6]
 [3,6] P21_GPIO >> <<P21 [3,4,6]
 [3,6] P22_GPIO >> <<P22 [3,4,6]
 [3,6] P23_GPIO >> <<P23 [3,4,6]
 [3,6] P24_GPIO >> <<P24 [3,6]
 [3,6] P25_GPIO >> <<P25 [3,4,6]
 [3,6] P26_GPIO >> <<P26 [3,4,6]
 [3,6] P27_GPIO >> <<P27 [3,4,6]
 [3,6] P28_GPIO >> <<P28 [3,6]
 [3,6] P29_GPIO >> <<P29 [3,4,6]

[3,6] P30_GPIO >> <<P30 [3,4,6]
 [5] NC1_CON >> <<NC1 [3,4,6]
 [5] NC2_CON >> <<NC2 [3,4,6]
 [5] P37_GPIO >> <<P37 [3,4,6]
 [5] P38_GPIO >> <<P38 [3,4,6]
 [5] P39_GPIO >> <<P39 [3,4,6]
 [5] P40_GPIO >> <<P40 [3,4,6]
 [5] P41_GPIO >> <<P41 [3,4,6]
 [5] P42_GPIO >> <<P42 [3,4,6]
 [5] P43_GPIO >> <<P43 [3,4,6]
 [5] P44_GPIO >> <<P44 [3,4,6]
 [5] P45_GPIO >> <<P45 [3,4,6]
 [5] P46_GPIO >> <<P46 [3,4,6]
 [5] P47_GPIO >> <<P47 [3,4,6]
 [5] P48_GPIO >> <<P48 [3,4,6]
 [5] P49_GPIO >> <<P49 [3,4,6]
 [5] P50_GPIO >> <<P50 [3,4,6]
 [5] P51_GPIO >> <<P51 [3,4,6]

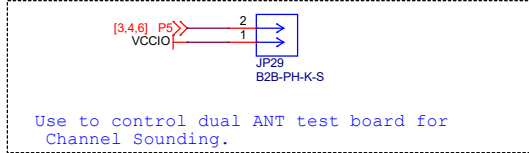
CONNECT SENSORS TO ATM3405 BGA



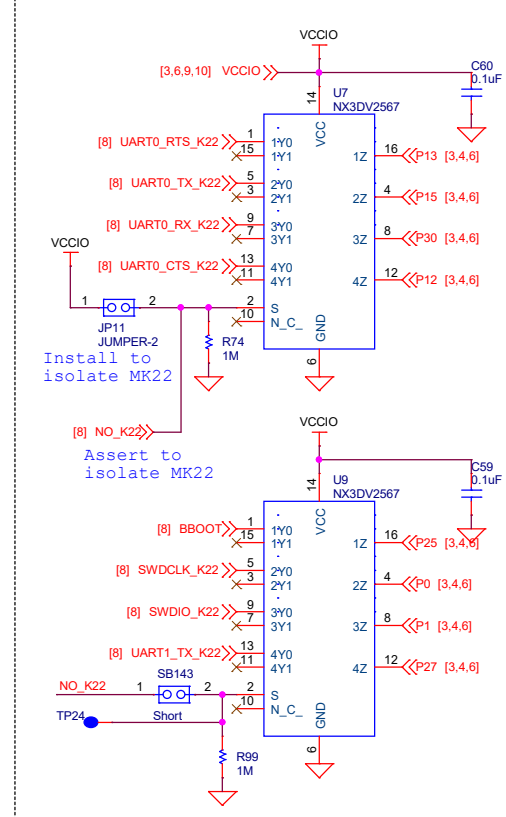
CONNECT LEDS/BUTTONS TO ATM3405 BGA



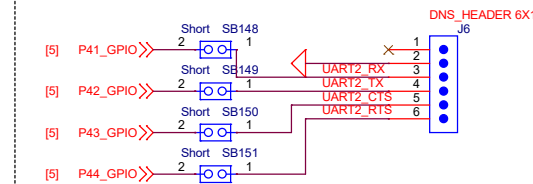
Control for Dual ANT Test Board



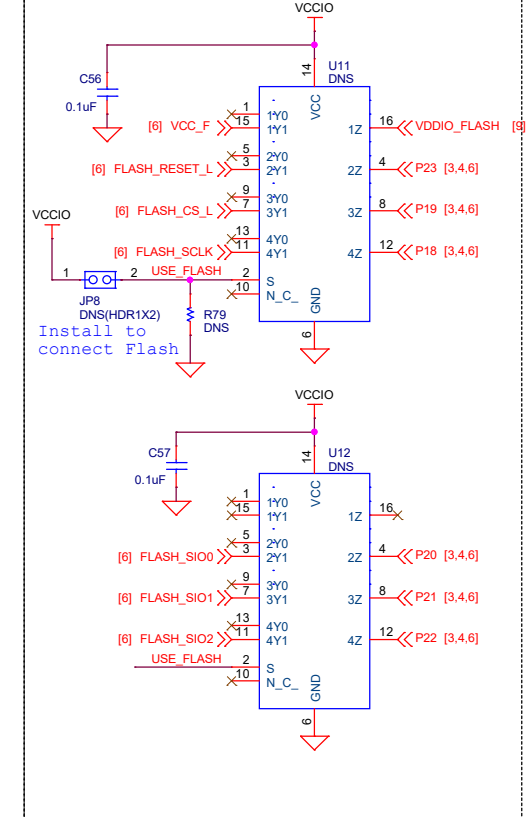
ISOLATE MK22 FROM ATM3405 BGA



Connected to external USB dongle for UART2

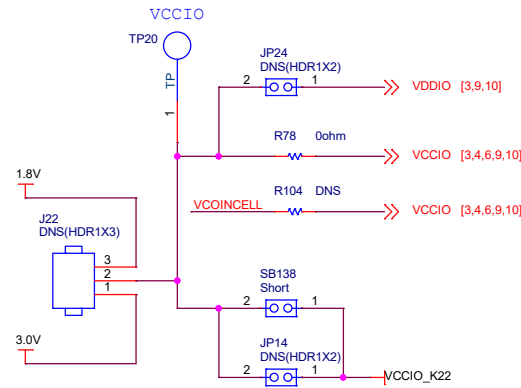
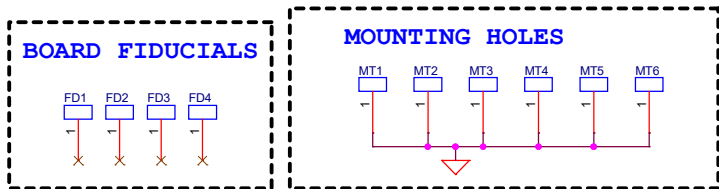
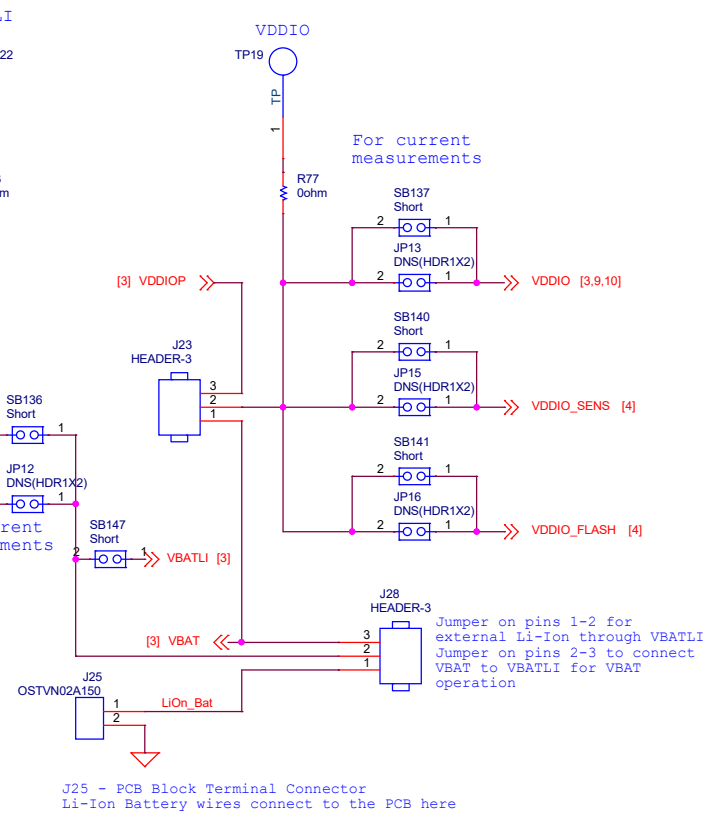
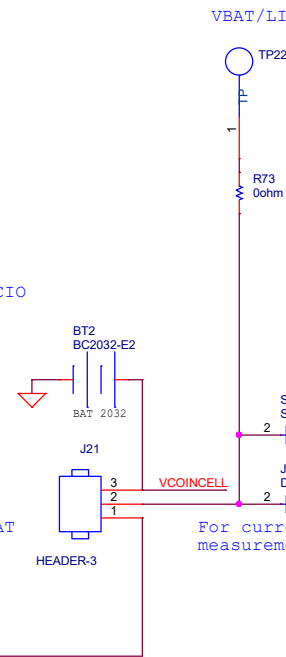
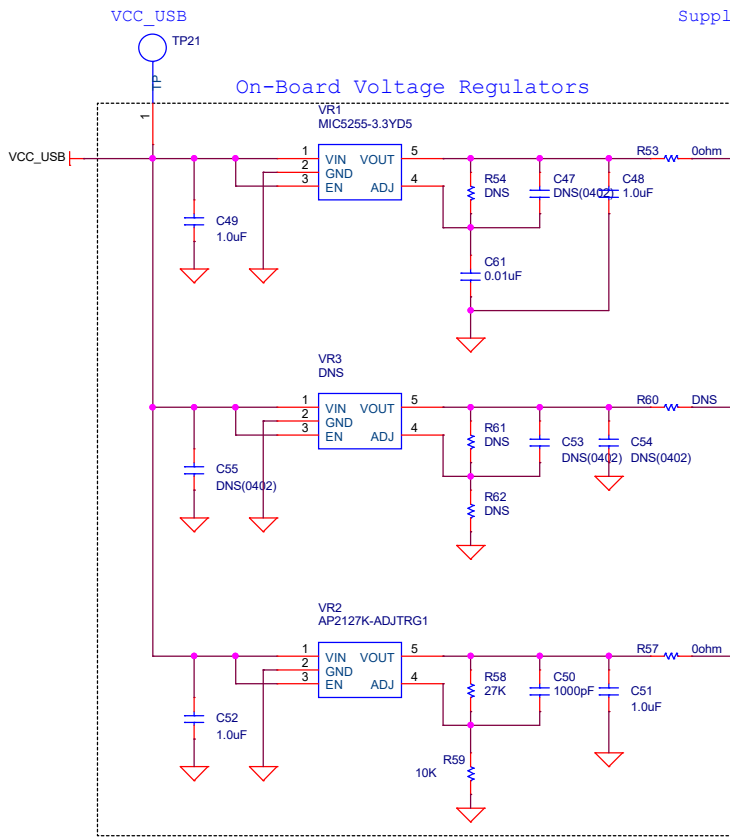


CONNECT FLASH TO ATM3405 BGA



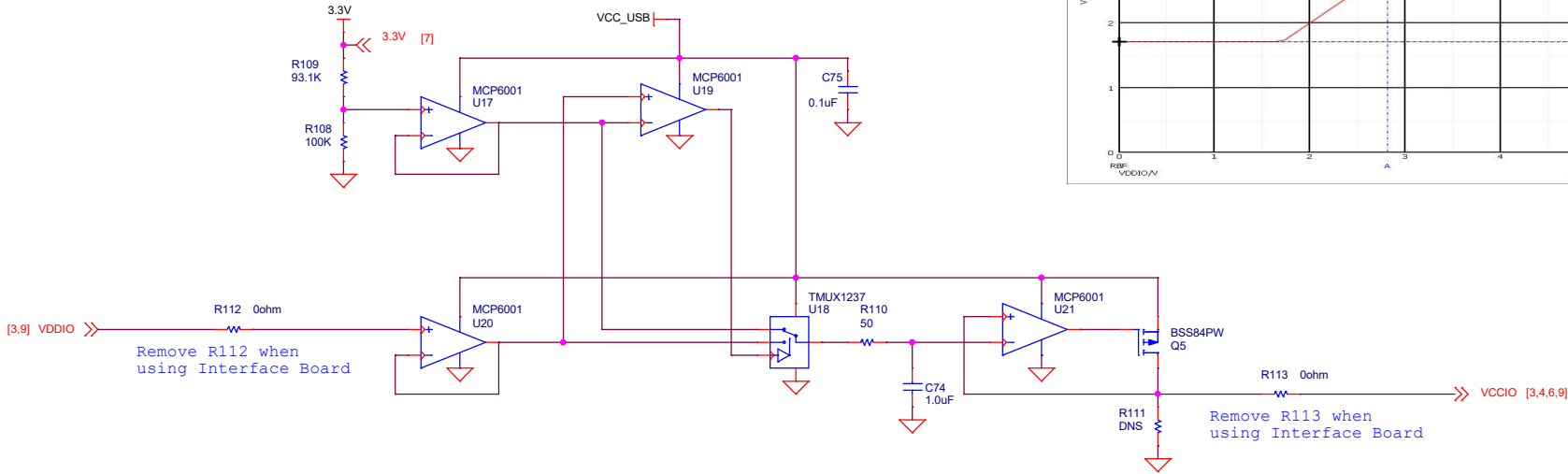
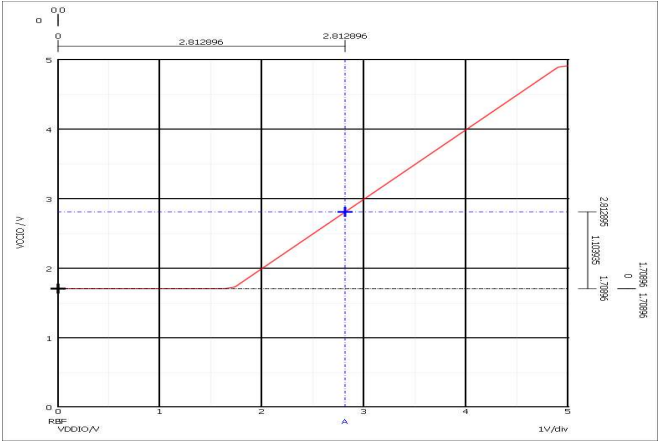
Atmosic Technologies Proprietary and Confidential

| ATMOSIC TECHNOLOGIES INC | | | |
|---|------------------------------|-------|--------|
| Title | | | |
| ATM3405 BGA Eval Board (JLink OB) - GPIO Mapping, Analog switches | | | |
| Size | Document Number | Rev | |
| B | 101-04-510-xxxx | 0.2 | |
| Date: | Wednesday, December 17, 2025 | Sheet | 4 of 8 |



| ATMOSIC TECHNOLOGIES INC | | | |
|---|------------------------------|--------------|---------|
| Title | | | |
| ATM3405 BGA Eval Board (JLink OB) - Power supplies and configurations | | | |
| Size B | | | |
| Document Number | 101-04-510-xxxx | | Rev 0.2 |
| Date: | Wednesday, December 17, 2025 | Sheet 7 of 8 | |

VDDIO < 1.72V: VCCIO = 1.71V
VDDIO >=1.72V: VCCIO = VDDIO



| | | | |
|--|------------------------------|-------|--------|
| Title | | | |
| ATM3405 BGA Eval Board (JLink OB) - VDDIO-VCCIO tracking circuit | | | |
| Size | Document Number | Rev | |
| B | 101-04-510-xxxx | 0.2 | |
| Date: | Wednesday, December 17, 2025 | Sheet | 8 of 8 |