Guidelines and Checklist for Board Designs with ATM33/e or ATM34/e Bluetooth SoC

SUMMARY: This guide provides a comprehensive, step-by-step workflow for designing the ATM33/e and ATM34/e BLE boards. It covers key topics such as schematic design, pin assignments, power management, test point planning, ESD protection, RF layout guidelines, and other critical PCB layout considerations. The goal is to support a smooth and efficient hardware development process.

Atmosic™

Guidelines and Checklist for Board Designs
With ATM33/e or ATM34/e Bluetooth SoC
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Acronyms and Abbreviations

Acronyms	Definition
ATM33/e	ATM3330e ATM3330 ATM3325
ATM34e	ATM3430e
ATM34	ATM3430 ATM3405
ATM34/e	ATM3430e ATM3430 ATM3405
EVB	Evaluation Board
EVK	Evaluation Kit
ESD	Electrostatic Discharge
PCB	Printed Circuit Board

1. Overview

This document serves as a comprehensive design and validation guide for engineers developing BLE hardware using the ATM33/e and ATM34/e series. It outlines best practices, critical design considerations, and verification checklists to support robust and efficient hardware development. This guide consolidates reference design knowledge, layout guidelines, and application-specific recommendations into a practical workflow to streamline the development process and improve first-pass success in hardware validation.

2. Design Phase

2.1 Schematic

- To begin the development process, please access the Atmosic Customer Portal and download the following materials:
  - Datasheet – Detailed technical specifications.
  - EVK (Evaluation Kit) and Reference Design HDK (Hardware Design Kit) – Includes schematics, layout, BOM, and Gerber files.
  - Hardware Design Guide – Comprehensive guidelines for designing.
  - Reference Manual – Technical documentation covering system architecture and functionality.
  - Pinmux Tool – A utility to configure and define pin assignments.
  - ESD Protection Application Notes – Recommendations for electrostatic discharge protection.
- Please refer to the HDKs from the reference design and Evaluation Board (EVB) as the starting point for development.
  - For schematic design, follow the hardware design guide to select appropriate components, such as 16 MHz and 32 kHz crystals, 3.3 uH switching inductor, harvester storage capacitor, and external flash.
- Pin Definitions.
  - Use the Pinmux Tool to identify and assign appropriate pins.
  - Select suitable pin assignments for all peripherals, including:
    - External Flash, LEDs, Buttons, Key Matrices, and other peripheral devices.

- Firmware Download, Debug Log, and RF Testing Signals.
  - Firmware Download: Uses P0(SWDCLK) and P1(SWDIO) for SWD to program the DUT.
  - Debugging: Utilizes P27 for UART1_Tx.
  - RF Testing via UART0: Supports DTM (2-wire) or HCI (2-wire or 4-wire) interface.
- Using a spreadsheet for all pin configurations in a spreadsheet. Figure 1 below is an example.

ATM3325 5x5 QFN, 2022/4/17									
PIN No.	Name	ADC	UWB	External Falsh	NFC	Sensor	Other	MP/Debug Request (Please reserve test points)	Descriptions
13	VBAT	ADC(Battery Voltage Monitor)							Battery Voltage Monitor
4	P0							SWDCLK	FW download
5	P1							SWDIO	FW download
7	P3			External Flash- Enable(Output)					External Flash- Enable(Output)
8	P4			External Flash- CS					External Flash- CS
9	P5		UWB-Ready(Intput)						UWB-Ready(Intput)
10	P6		UWB-INT(Intput)						UWB-INT(Intput)
11	P7		UWB-RST(Output)						UWB-RST(Output)
24	P12		UWB-CS						UWB-CS
25	P13		UWB-CLK	External Flash- CLK					UWB,External Flash-CLK,
26	P14		UWB-MO	External Flash- MO					UWB,External Flash-MO
27	P15		UWB-MI	External Flash- MI					UWB,External Flash-MI
29	P17				NFC-FD(Intput)				NFC-FD(Intput)
30	P18				NFC-I2C_CLK	Sensor-I2C_CLK			NFC,Sensor-I2C_CLK
31	P19				NFC-I2C_DATA	Sensor-I2C_DATA			NFC,Sensor_DATA
32	P20				NFC-I2C_Vdet(Output)				NFC-I2C_Vdet(Output)
33	P21							UART0_TX	MFG/RD Test CMD
34	P22							UART0_RX	MFG/RD Test CMD
35	P25						Buzzer(Output)	BBOOT	BBOOT needs to be co-used with Buzzer. Default low
38	P27							UART1_TX	System debug log
39	P29						BTN_Button(Input)		BTN_Button(Input)
40	P30					Sensor-INT(Input)			Sensor-INT(Input)
12	PWD							PWD	Power Down and reset. High active.

Figure 1 - Pin configurations in a spreadsheet

- Power-related connection.
  - Refer to the Reference Manual to determine an appropriate power scheme for your design.
  - If integrating third-party devices, ensure that:
    - The voltage levels and current drive capability of the external devices are compatible with the ATM33/e or ATM34/e device.
    - The pin limitations of both the chipset and peripherals are considered to avoid conflicts.
    - Provisions are included for isolating the power supplies of external devices from the ATM33/e or ATM34/e to facilitate debugging.
  - For each power input and output pin, adhere to the capacitor specifications recommended in the EVK or reference design and follow the recommended capacitor values and materials to ensure power stability and noise reduction.
  - Consider the battery, energy harvesting circuits, charging circuits, and reset circuits.
  - For the first design, reserve a series 0 resistor in the main power path (VBATLI/VBAT).

- Check and confirm digital connections and place suitable test points for testing requirements, including VBATLI/VBAT, VDDIO, PWD, BBOOT(P25), UART0, UART1_TX, and GND.

2.1 Layout

- If the board is a two-layer board, it's recommended that the board is as thin as mechanically possible to minimize the width (to save space on the PCB as well as to minimize discontinuities between trace and component pads) of the 50 Ω transmission line between the RFIO pin of the Atmosic device and the antenna, as well as to minimize the chances for unintended RF radiation from high impedance traces not having proper GND close by.
- If the board is a two-layer board, make sure the 50 Ω transmission line connecting the RFIO pin and the antenna and other critical analog traces, such as the analog 1.0 V core supply, are routed with proper ground return paths close by. For the 50 Ω transmission line, there should be well grounded continuous copper immediately underneath, large enough to form a proper microstrip structure. For the analog 1.0 V core supply, make sure continuous ground copper is running along the entire trace to provide a good current return path. Also, make sure this trace is closer to the ground than any nearby traces.
- If the board is a four-layer board, it's recommended to use the top layer for RF traces and most of the routing, and the second layer as a solid ground. It is also recommended to minimize the thickness of this top-layer-to-second-layer core to keep trace widths small (save room on PCB and minimize discontinuities between trace and component pads) as well as reduce chances for unintended RF radiation.
- For placement, it is recommended to place the Atmosic device as close to the antenna as possible to minimize needless board loss (resulting in lower transmit power efficiency and worse receiver sensitivity), to preserve the integrity of the transmission line, and to prevent potential radiation of harmonics.
- Antenna matching components should be as close to the antenna as possible, and all the matching components should be placed as close to each other as possible, connected by traces that have widths matching the component pad widths. Similarly, the RFIO matching network, including the DC blocking capacitor, should be as close to the RFIO pin as possible, and all the matching components should be placed as close to each other as

possible, connected by traces that have widths matching the component pad widths. The transmission line connecting the RFIO matching network and the antenna matching network should be 50 Ω.

- Each grounded component should have at least one (more is better) ground via of its own, not sharing the via with another component. This ground should be directly connected to the ground of the Atmosic device with the least inductance and resistance possible.
- The decoupling capacitors for the various supply rails should be placed as close to the corresponding Atmosic device pins as possible (for the Atmosic devices in QN, QK, and LQK packages). For the CM package, the decoupling capacitor for AVDD1P is recommended to be approximately 10mm in trace length away from the pin.
- The 16 MHz crystal should be as close as possible to the Atmosic device. The two traces connecting it to the Atmosic device should form the smallest loop area possible. Placing it farther away increases the risks of higher 16 MHz spurs, which can potentially affect receiver sensitivity and radiated harmonics.
- The switching regulator inductor should be as close as possible to the Atmosic device, with its traces forming the smallest loop area possible to minimize switching noise affecting the receiver sensitivity. The two connecting traces also need to be as wide as possible to reduce the ohmic loss, resulting in higher power consumption. This inductor should also be kept away from the AVDD1P trace and decoupling capacitor.
- The RC filter for the analog 1.0 V core supply AVDD1 should be placed as close to the AVDD1 pin as possible.
- The AVDD1-AVDD1P trace should be kept away from noisy digital traces running parallel or crossing under it.
- Copper pours should be grounded with vias that are no greater than 1.5cm apart.
- For the 7x7 or 5x5 QFN package, make sure the center ground pad is well grounded with as many vias as physically possible.

3. Checklist

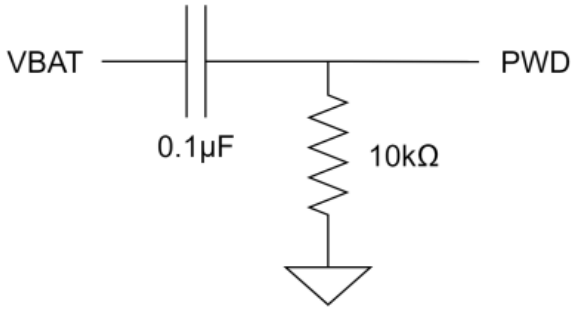
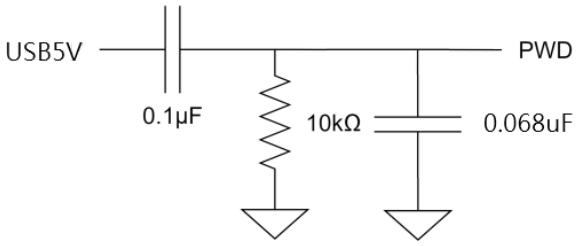
3.1 Schematic Checklist

3.1.1 PMU

Item	Check ☐ **Indicates checkboxes for verifying items, making it easier to review and confirm the board design.**
VBATLI(Input) **VBAT(Input)**	☐ For voltage levels greater than 3.3 V, VBATLI must be used, and VBAT must be connected to a bypass capacitor (10 µF) and can't be used to power other peripherals. VBATLI must be between 2.7 V and 4.2 V, and recommended to be greater than or equal to 3.6 V. ☐ For voltage levels between 1.1 V and 3.3 V, VBAT should be used and should also be connected to VBATLI.
VDDIOP(Output) **VDDIO(Input)**	☐ VDDIOP must be connected to a bypass capacitor. ● For ATM33/e, VDDIOP bypass capacitor (default 1µF). For ATM34/e, VDDIOP bypass capacitor (default 4.7µF). ☐ If VBAT is used. ● Recommend connecting VDDIO to VDDIOP for the I/O supply internally generated at 1.8 V. ● If VBAT is between 1.1 V and 1.8 V, the I/O supply must be internally generated. ● The ATM33/e can power peripherals using its internally generated I/O supply, supporting up to an average of 50 mA. If the combined current consumption of all peripherals exceeds this value, an external I/O supply is required. ● The ATM34/e supports up to an average of 25 mA from its internal I/O supply. Similarly, if the peripheral current exceeds this limit, an external I/O supply should be used. **Note**: The ATM33/e, ATM34/e PMU can sustain a maximum average load of 100 mW (measured at

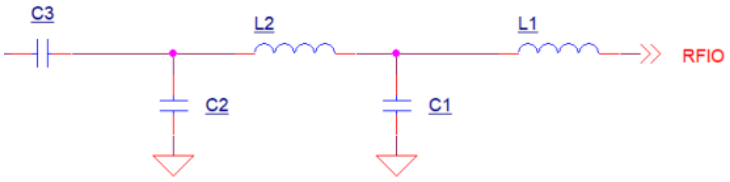
	VBAT), which includes the ATM34/e as well as any peripherals that are being powered. ☐ If VBATLI is used, then VDDIO must not be connected to VBAT. ● Recommend connecting VDDIO to VDDIOP for the I/O supply internally generated at 1.8 V. ● The ATM33/e, ATM34/e can sustain a maximum of 0.5mA from its internally generated I/O supply during low power states. If the combined current consumption of all peripherals can exceed this value while the ATM34/e is in a low-power state, an external I/O supply is needed. ● If the I/O supply needs to be between the supported range of 1.8V to 3.3V for any reason, including peripheral requirements, an external source can be used to supply the I/O rail. In this case, do not connect VDDIOP to VDDIO, and connect VDDIO to the external source. ☐ Make sure bypass capacitors of at least 1 µF are placed as close to each of the VDDIOP and VDDIO pins.
DVDD1P(Output) **DVDD1(Input)** **AVDD1P(Output)** **AVDD1(Input)**	☐ Must connect DVDD1P to DVDD1, with bypass capacitors of 10 µF and 1µF placed as close to the respective pins. ☐ Must connect AVDD1P to AVDD1 via the RC filter. ● AVDD1P with bypass capacitors of 10 µF. ● For ATM33/e: ○ RC filter (1 Ω + 10uF) close to the AVDD1. ○ If the 10 dBm TX setting is used or the solution will be used in cold temperatures (< -10°C), the AVDD1 bypass capacitor needs to be increased to 22 µF instead of the 10 µF bypass capacitor. ● For ATM34/e: ○ RC filter (1 Ω + 20uF(2 0402 10uF) or 22uF 0603) close to the AVDD1.

VDDPA(Input)	☐ When the maximum TX output power is 4 dBm or lower, then it is recommended to connect VDDPA to one of the following options. ● VDDIOP. ● A bypass capacitor of 1 µF. Do not connect VDDPA to the ground. Floating VDDPA is also a possibility, but not recommended. ☐ For ATM33/e, ATM34/e, when TX output power is greater than 4 dBm (6 dBm, 8 dBm, or 10 dBm), VDDPA must be connected to VDDIOP with a 1 µF bypass cap placed as close as possible to the VDDPA pin. ☐ For ATM33/e, if VDDIOP is loaded with greater than 3 mA average loads and is also connected to the VDDPA pin, the receive sensitivity may be impacted depending on the specific board layout. If this issue is seen, we recommend adding a series inductor or ferrite bead in series between VDDIOP and VDDPA and close to the VDDPA bypass cap. On the ATM33/e EVB, this issue is resolved using a 120 nH inductor in series to the bypass capacitor at VDDPA.
VAUX(OUTPUT)	☐ VAUX is used internally by the PMU. It is not supported for use by other peripheral devices. ☐ The bypass capacitor must be 4.7 µF.
Power On Reset **USB Charger Reset**	☐ Power Down (PWD) should be pulled low to allow for debug and production test support. Pulses of voltage greater than 0.7 V and greater than 1 ms in duration are required when this pin is used for resetting the device. ☐ For applications where the primary power source can be disconnected or experience large voltage fluctuations for short periods, a PWD circuit in Figure 2

	below is required to ensure the reset is performed properly.  Figure 2 - PWD circuit ☐ If a charger reset is required for a 5V USB charger, the following Figure 3 PWD circuit is recommended to ensure a proper reset.  Figure 3 - 5V USB charger reset circuit

3.1.2 RF and Crystal

Item	Check ☐ **Indicates checkboxes for verifying items, making it easier to review and confirm the board design.**
Antenna and Antenna matching components	☐ If a chip antenna is used, it is recommended to use one with a shorted stub to GND (for extra ESD protection of the RFIO pin). There needs to be sufficient GND copper clearance around the antenna. ☐ If a PIFA is used, there's a built-in shorted stub to GND in the antenna, so an ESD diode is not needed. ☐ The 2 or 3 matching components should be right at the antenna feed. ☐ If the antenna used does not provide a DC short to GND, it is prudent to have a placeholder for a small shunt ESD

	diode right next to one of the shunt antenna matching components.
RFIO matching circuit	☐ The Figure 4 RFIO matching circuit comprises 2 series inductors and 2 shunt capacitors. And there's an additional DC block series capacitor connecting this RFIO matching circuit to the antenna matching circuit.  Figure 4 - RFIO matching circuit
16 MHz Crystal	☐ The ATM33/e, ATM34/e can support load capacitance up to 12 pF with internal tuning capacitors, but < 9 pF is recommended for lower power consumption. ☐ The 16 MHz crystal used on the ATM33/e, ATM34/e EVB is the E1SB16E00001KE from Hosonic (+/-10 ppm tolerance, +/-15 ppm stability, 8 pF load capacitance, 80 Ω maximum ESR). ☐ This can be used as a reference when choosing alternate parts (e.g., Epson FA-20H 16.0000MF20X-AJ or ECS ECS-160-8-36-JTN). ☐ There is no need to place two external load capacitors by default. If load capacitors must be included in the design, please provide placeholders only—do not populate them with any capacitors initially.
32.768KHz Crystal	☐ The ATM33/e, ATM34/e can support load capacitance up to 12 pF with internal tuning capacitors, but < 9 pF is recommended for lower power consumption. ☐ The 32.768 kHz crystal used on the ATM33/e, ATM34/e EVB is the SC20S-7PF20PPM from Seiko Instruments (+/-20 ppm tolerance, 7 pF load capacitance, 70 kΩ maximum ESR). ☐ This can be used as a reference when choosing alternate parts (e.g., Micro Crystal AG CM8V-T1A-32.768KHZ-7PF-100PPM-TA-QC). ☐ If the application does not require a crystal, the XTALI_32k pin should be grounded, and the XTALO_32k pin should be left floating. ☐ If the design requires an option to support configurations with or without a 32 kHz crystal, please add a 0201 placeholder (footprint) between the XTALI_32k pin and ground. When the application does not require a crystal,

	populate this placeholder with a 0 Ω resistor to short XTALI_32k to ground. ☐ There is no need to place two external load capacitors by default. If load capacitors must be included in the design, please provide placeholders only—do not populate them with any capacitors initially.

3.1.3 Interface

Item	Check ☐ **Indicates checkboxes for verifying items, making it easier to review and confirm the board design.**
I2C	☐ When the I2C interface is used, please make sure there is a pull-up resistor (10 kΩ) option on the SDA and SCK path. ☐ Please check the pinmux to make sure the GPIO is available for I2C.
PDM/PCM/KSI/KSO	☐ Please check the pinmux to make sure the GPIO is available

3.1.4 Debug Message and Production Test Points

Item	Check ☐ **Indicates checkboxes for verifying items, making it easier to review and confirm the board design.**
Test Points	☐ VBAT or VBATLI ☐ GND ☐ PWD ☐ P25(BBoot) ☐ P0 and P1 (SWD) ☐ UART0_TX/UART0_RX /UART0_CTS(optional)/ UART0_RTS(optional)

	● UART0 for RF testing via DTM (2-wire) or HCI (2-wire or 4-wire) interface ☐ UART1_TX(default P27) ● Debug message
FFC Connector	☐ The connector used for FW programming on the engineering side. Please reserve the connector if there is no size concern.
Pull Down Resistor	☐ P25 ● A weak 100 kΩ pull-down resistor is required. ☐ PWD ● A pull-down resistor is required; the default is 1 MΩ. ● If using a power-on reset circuit or a USB charger reset circuit, PWD uses a 10 kΩ pull-down resistor.

3.2 Layout Checklist

Item	Check ☐ **Indicates checkboxes for verifying items, making it easier to review and confirm the board design.**
Antenna	☐ If a chip antenna is used, it is recommended to use one with a shorted stub to GND (for extra ESD protection of the RFIO pin). There needs to be sufficient GND copper clearance around the antenna. ☐ If a PIFA is used, there's a built-in shorted stub to GND in the antenna, so an ESD diode is not needed.
Antenna matching components	☐ These 2 or 3 components should be right at the antenna feed, where the GND copper starts/stops. These components convert antenna impedance to 50 Ω. ☐ The components should be placed tightly together, with the shortest trace lengths possible between them. ☐ The trace connecting these components need not be 50 Ω. Their widths can be the same as the width of the component footprint pads to minimize discontinuities. ☐ The shunt components should be well grounded using the biggest possible vias (no more than 1mm away) and grounded to copper that has the shortest possible paths back to the ground of the Atmosic device.

	☐ If the antenna used does not provide a DC short to GND, it is prudent to have a placeholder for a small shunt ESD diode right next to one of the shunt antenna matching components.
Trace connecting antenna matching circuit to the RFIO matching	☐ The impedance of this trace needs to be 50 Ω. This trace can be implemented as a microstrip or co-planar WG structure, depending on the thickness of the PCB and the availability of the GND copper on both layers. ☐ It is important that the integrity of this structure be maintained throughout its entire length, with no interruption of the GND copper by other traces, and that the GND copper has 0 inductance connection to the GND of the Atmosic device. ☐ It is best to keep this 50 Ω transmission line as short as possible to minimize loss. That's why it is recommended that the Atmosic device be located as close to the antenna as physically possible.
RFIO matching circuit	☐ The RFIO matching circuit comprises 2 series inductors and 2 shunt capacitors. And there's an additional DC block series capacitor connecting this RFIO matching circuit to the antenna matching circuit. ☐ The first series inductor needs to be as close (less than 1.5mm) to the RFIO pin as physically possible. ☐ Then the first shunt cap needs to be as close as physically possible to that first inductor, with the shortest trace possible connecting them. This trace does not need to be 50 Ω, but it should not be bent sideways or back. Similarly, for the next series, inductor and shunt cap. ☐ All four matching components need to be tightly grouped together and closest to the RFIO pin. ☐ Finally, the DC block series cap can be anywhere between the RFIO matching circuit and the antenna matching circuit. ☐ One important thing to pay attention to is that the two shunt capacitors need to be well grounded, using low inductance vias closest (no more than 1 mm) to the capacitor possible. And each shunt capacitor should have its own two GND vias. These two shunt capacitors cannot share the same GND vias..
The center GND pad under the Atmosic device	☐ This pad is the only GND connection between the Atmosic device circuitry and the circuitry on the PCB. It is very important to make sure there's a very low inductance connection between this pad and the GND copper of the

	PCB using lots of GND vias, as many as physically possible. ☐ The GND PCB copper under this pad (on the opposite layer) can be broken by a trace if necessary, as long as there are enough GND vias to provide a low inductance connection. ☐ Any unused Atmosic device pins that can be grounded should be grounded to this center pad to help improve the GND copper connection on the PCB layer of the Atmosic chip.
AVDDPA pin	☐ This pin needs a 1uF decoupling cap as close (less than 2mm) as possible. ☐ Keep the route to this pin short and near GND return if possible to minimize unwanted radiation of harmonics.
AVDD1 pin	☐ This is the 1.0 V input supply for the analog and RF circuitry in the Atmosic chip, so it has to be very clean. This 1.0 V comes from the internal switcher 1.0 V output AVDD1P after an RC filter. ☐ It is very important to place the RC filter as close (less than 3mm) as possible to the AVDD1 pin so that the filter can also filter out any additional noise that may get picked up along the trace connecting AVDD1P. ☐ The resistor and capacitor need to stay together near the AVDD1 pin.
AVDD1P trace	☐ This trace brings the 1.0 V output from the internal switcher at pin AVDD1P to the AVDD1 input pin. ☐ It is very important to shield this trace from all noise sources because this 1.0 V powers the analog and RF circuitry inside the Atmosic device. This means avoid having this trace running parallel or close to an active digital trace, either on the same layer or on the adjacent layer. ☐ In addition to shielding the trace from noise, it is also good for the trace to have a nearby GND return path.
AVDD1P pin	☐ This pin needs to connect first to a close by 10 uF decoupling capacitor before it goes to a via to the AVDD1P trace. This ensures that most of the switching noise is shorted to GND before it has a chance to get onto the trace going to the AVDD1. ☐ The closer the 10 uF is to the pin, the better the switcher efficiency and the lower the switcher noise.

Switcher inductor	☐ Place this inductor as close (less than 3 mm) to the Atmosic device as possible and minimize the loop area formed by the Atmosic device and the inductor by keeping the two connecting traces short and close to each other. ☐ Make the connecting traces as wide as possible to reduce resistive loss ☐ Keep the inductor and the Atmosic device on the same layer to avoid via losses. ☐ Keep the AVDD1P trace and decoupling capacitor away from this inductor.
16 MHz Crystal	☐ Keep this crystal close to the Atmosic device and minimize the loop area formed by the crystal and the Atmosic device by keeping the two connecting traces short and close to each other. ☐ Keep the AVDD1P trace away from this crystal and connecting traces.
Decoupling capacitors for VDDIOP, AVDD1P, VAUX, DVDD1P, VBAT	☐ Place these capacitors as close (less than 2 mm) to their respective pins as possible, with higher priority given to AVDD1P and VBAT, and lowest priority for VAUX. ☐ It is very important for each of these capacitors to have its own via and direct path to GND, especially AVDD1P and VBAT. These should not be connected and share the same vias or have a common high inductance path to GND with VAUX and DVDD1P, and VDDIOP.
Non-critical components	☐ These are components related to the PWD, P25, and 32 kHz crystal. They can be placed farther away from the Atmosic device to make room for the critical components.
Power routes	☐ VBAT trace carries the most current and can be made wider (15 mils or greater) if there's PCB room, and can be made thinner (10 mA) on a small board where it does not run very far, if PCB space is limited. ☐ All other power traces (AVDD1P, DVDD1P, VDDIOP, AVDDPA) don't carry much current and are not lengthy, so they don't need to be thick (10 mils or less) if PCB space is limited..

3.3 Robust Design for ATM3405-5YCABV (Perth 4x4 BGA)

Item	Check ☐ Indicates checkboxes for verifying items, making it easier to review and confirm the board design.
Schematic design	☐ Decoupling capacitors for all voltage supply rails generated by the ATM3405 should have the same values recommended by the reference design ☐ RFIO matching component values and manufacturers should be as recommended by the reference design (only TDK MHQ series inductors, or Murata LQP0xHQ series inductors should be used) ☐ Power inductor connected to LEXT1/LEXT2 should have the lowest DCR possible and the highest saturated current possible, as recommended by the reference design
PCB stackup	☐ Minimum layer count: 6 ☐ The top layer is used for fanning out outer-row balls, including RFIO (A1) ☐ Layer 2 is used for fanning out inner-row balls using micro blind vias (L1-L2) placed between the inner row and GND balls ☐ Layer 3 is the GND plane ☐ Layer 4 and Layer 6 routing ☐ Layer 5 mostly GND reference for Layer 6 ☐ L1-L2 and L2-L3 substrates should be thin (3- 5 mils) for good GND reference, low GND inductance, and more reliable (L1-L2) micro vias
ATM3405 grounding	☐ Center 25 GND balls are grounded using a combination of L1-L2 blind micro vias and L2-L5 standard buried vias to avoid in-pad vias
Decoupling capacitors	☐ Decoupling capacitors for supply rails VBAT, AVDD1, VDDIO, VDDPA, AVDD1P, DVDD1P, VAUX, and VDDIOP should be placed as close to their balls as possible, with the widest possible connecting traces to minimize inductance and resistance ☐ These decoupling capacitors should not share GND vias. Each capacitor should have its own GND via. ☐ Power inductor connected to LEXT1 and LEXT2 should be placed as close to the balls as possible, with the widest possible traces possible and both traces and the

	inductor should be kept as isolated as possible from the supply traces and decoupling capacitors.
RFIO matching components	☐ Matching components should be placed as close to ball A1 as possible ☐ The spacing between each matching component should be as small as possible ☐ The alignment of the matching components should be linear and sequential, extending straight away from A1 toward the antenna ☐ Grounding for each shunt component should be done with vias as large as possible to reduce inductance ☐ Other components and traces should keep a distance from these matching components
Antenna matching components	☐ Antenna matching components should be placed as close to the antenna as possible, and as tightly grouped together as possible ☐ If the antenna is not DC shorted to GND, it is recommended to include a shunt ESD diode on the RFIO path, near the antenna ☐ The trace connecting the antenna match and the RFIO match should have an impedance of 50 Ω and be kept as short as possible, without interruption in the GND plane underneath.
1.0 V analog supply (A2)	☐ This AVDD1 input gets its 1.0 V supply from AVDD1P (ball L9), after an RC filter to suppress switching noise ☐ The RC filter components should be placed close to ball A2 ☐ The trace connecting AVDD1P to the RC filter should begin from the decoupling cap, should be short, kept away from other traces, the crystal, and the switching inductor, and have a good ground return
Crystals	☐ A 16 MHz crystal should be placed as close as possible to the ATM3405 ☐ A 32 kHz crystal can be placed further away if needed

Reference Documents

Title	Document Number
ATM33e Series Datasheet	ATM33e-DS-xxxx
ATM33/2 Series Hardware Design Guide	ATM33_e-DGHW-xxxx
ATM34/e Series Datasheet	6494-xxxx-xxxx
ATM34 Series Hardware Design Guide	6448-xxxx-xxxx
ATM34/e Series Reference Manual	6444-xxxx-xxxx
ESD Protection Application Note	7812-xxxx-xxxx

Revision History

Date	Version	Description
June 30, 2025	0.10	Initial version created.

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