ATM34/e ROM UART Bootloader

Application Note

SUMMARY: This document describes the ROM UART bootloader operation for the ATM34/e Wireless SoC Series.

Atmosic™

ATM34/e Series ROM UART Bootloader Application Note
Nov 25, 2025
9723-0219-0050

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Acronyms and Abbreviations

Acronyms	Definition
ATM34/e	ATM3430e ATM3430 ATM3405
SoC	System-on-Chip

1. Overview

This document describes the ROM UART Bootloader operation and requirements for the ATM34/e Wireless SoC Series. This ROM UART Bootloader mode is intended to allow updating code into the ATM34's RRAM or Flash when the ATM34 device has never been programmed. ROM UART Bootloader mode is also applicable to the ATM34 devices that have been programmed. This enables the ATM34/e device to boot, load code into SRAM, and continue executing code. The traditional way was to use SWD to program the device. This enables the ATM34/e device to boot, load code into SRAM, and continue executing code.

2. Hardware and Software Requirements

2.1 Supported EVKs

This document applies to:

EVK	SoC Package	SoC Part Number	Kit Part Number
Evaluation Kit for ATM3430e 7x7 QFN	56-pin 7x7 mm QFN	ATM3430E-5YCAQN	ATMEVK-3430e-YQN-5
Evaluation Kit for ATM3405 BGA	93-ball 4x4 mm BGA	ATM3405-5YCABV	ATMEVK-3405-YBV-5
Evaluation Kit for ATM3405 5x5 QFN	40-pin 5x5 mm QFN	ATM3405-5WCAQK ATM3405-5PCAQK	ATMEVK-3405-WQK-5

Table 2-1 - Supported ATM34/e Series EVKs

2.2 Supported Software

Please use the latest Atmosic OpenAir release at https://github.com/Atmosic/openair.

The ROM UART Bootloader tool package is available in Python scripts and Windows executables, and can be found at https://atmosic.com/software-utilities. For detailed usage, refer to the README.md files in the respective directories.

3. ROM UART Bootloader

ROM UART Bootloader functionality allows a connected host over UART to download executable images using the Xmodem-1K protocol into ATM34's SRAM. The downloaded image loaded into the SRAM can, in turn, initiate the FW download procedure with the attached host over UART.

3.1 ROM UART Bootloader Basic Operation

P25 (BBOOT/UART1 RX) and P27 (UART1 TX) are mandatory pins for the ROM UART Bootloader functionality.

Upon powering on or asserting the PWD signal, ROM monitors the BBOOT (P25) state. BBOOT assertion is active high.

- If the BBOOT state is low, ROM continues the normal boot sequence.
- If the ROM detects the BBOOT pin high, it monitors for 10 state transitions on P25 to activate the ROM UART Bootloader mode, as shown in the timing diagram below.
    - The host can initiate 10 state transitions by sending a character 'U' (Hex: 0x55) over the host UART TX (ATM34 UART1 RX) line.
    - Once activated, ATM34 ROM reconfigures BBOOT P25 as ATM34 UART1 RX and P27 as ATM34 UART1 TX. ROM sets the baud rate to 115200 bps, initiates Xmodem-1K protocol, and waits for the first Xmodem-1K protocol header from the host.
    - The host can initiate Xmodem-1K data transfer to load code into SRAM for execution.
    - Once the Xmodem-1K transfer is successful, the ROM starts executing code that was loaded into SRAM.

3.2 Security

ROM UART Bootloader feature can be disabled by programming EFUSE/OTP bit 56 (Refer to the atm_otp driver in the openair repository mentioned above). Once this bit is set, UART1 RX capability is disabled in hardware.

For recovery, the application and/or bootloader can unlock the ROM UART Bootloader functionality via a higher-layer authentication mechanism if needed.

3.3 Hardware Design Circuitry Requirements

Different approaches are possible depending on the requirements of the Host PC/Test JIG.

Option#1	Allow the fixture to run as a development platform to either boot normally or boot into ROM UART Bootloader mode
Option#2	Always boot into ROM UART Bootloader mode on power up

Table 3-1 - Design Options for Supporting ROM UART Bootloader Mode

3.3.1 Option#1: Separate BBOOT (P25) and UART1 RX (P25) on Host Side

Supporting ROM UART Bootloader mode requires additional hardware circuitry if the goal is to retain the flexibility to run in normal mode of operation. This hardware circuitry is already built into the ATM34 EVKs listed above. The BBOOT functionality is shared with the UART1 RX functionality. This circuitry is mandatory for customers who wish to support the capability to load software for the first time and require it to operate in the normal boot sequence after the programming. This circuit can be implemented directly on the main board or added via an external module.

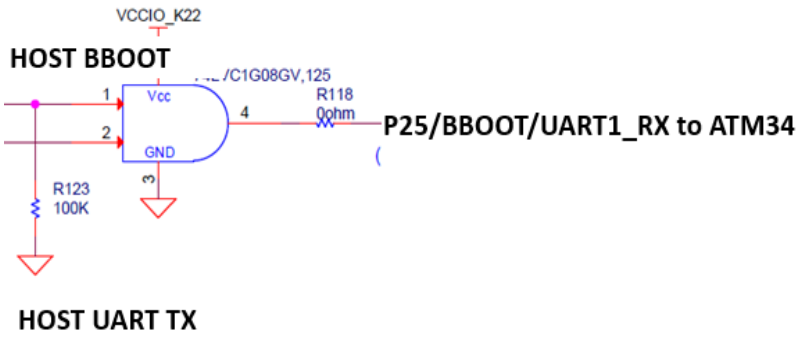

Figure 3-1 - Mandatory Circuitry for Option #1 - Separate BBOOT (P25) and UART1 RX (P25)

The timing diagram below shows the input/output of the AND gate and the sequence required to get into the ROM UART Bootloader mode. This diagram does not show the ATM34 UART1 TX responses.

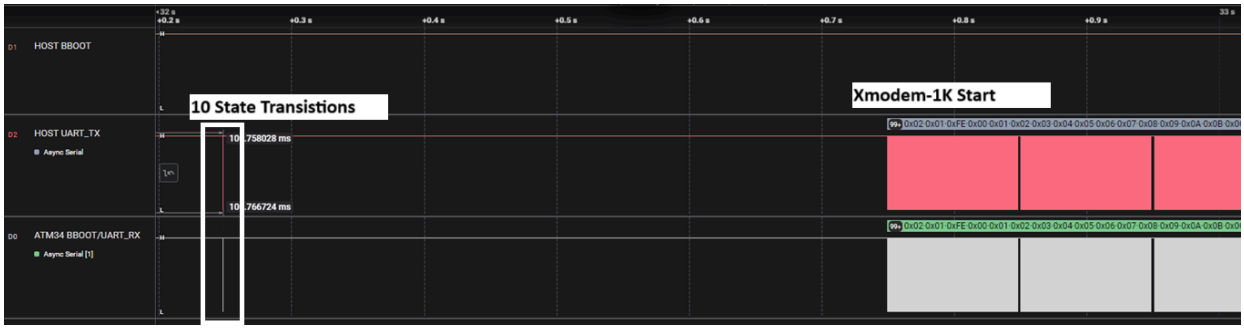

Figure 3-2 - Timing Diagram for Option #1 - Separate BBOOT (P25) and UART1 RX (P25)

Zoomed in on the 10 state transitions needed to switch from BBOOT to UART1 RX mode and enable Xmodem-1K protocol reception.

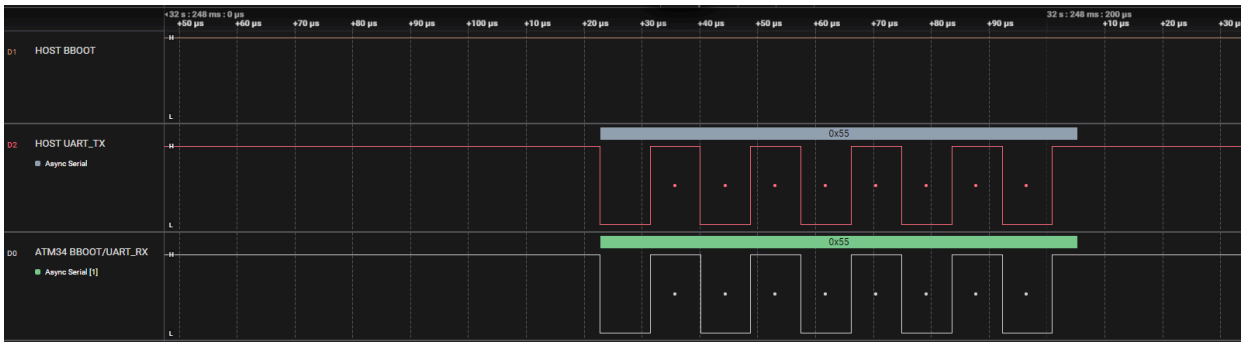

Figure 3-3 - Timing Diagram for Option #1 - Zoom in on 10 State Transitions

Zoomed in on the start of Xmodem-1K protocol.

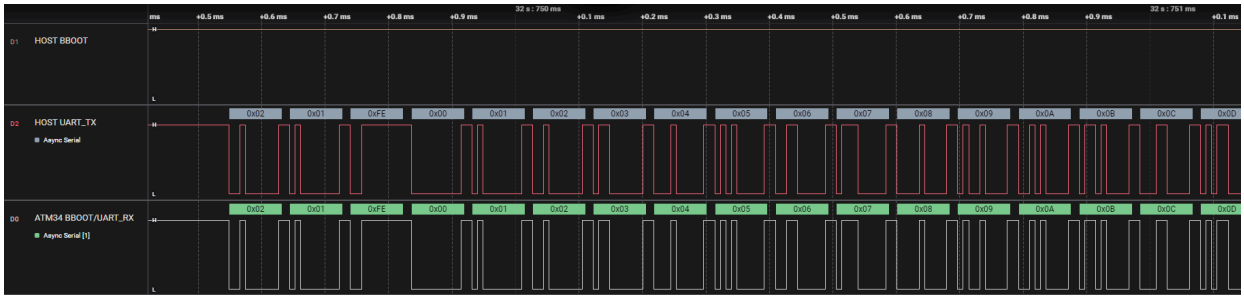

Figure 3-4 - Timing Diagram for Option #1 - Zoom in on Start of Xmodem-1K Protocol

3.3.2 Option#2: Shared BBOOT (P25) and UART1 RX (P25) Signal on the Host Side

In this implementation, the BBOOT signal shares the same line as Host UART TX (ATM34 UART1 RX); the ATM34 powers on in BBOOT mode by default. This happens because the UART line idles high, which activates BBOOT. For this option, no additional hardware circuitry is required.

As a result, if code is already present in RRAM, the device will not follow the normal boot sequence (see Section 3.1). To enable normal booting after programming, the BBOOT signal must be deasserted. Then, when PWD is triggered, the ROM samples BBOOT low and proceeds with the normal boot sequence.

Similar to Option#1, ATM34 will monitor 10 P25 state transitions to activate the ROM UART Bootloader mode, as shown in the timing diagram below. The rest of the sequence is identical to before.

The timing diagram below shows the power-on (Host UART connected to ATM34), the default state of the pin signals, and the sequence needed to enter the ROM UART Bootloader mode.

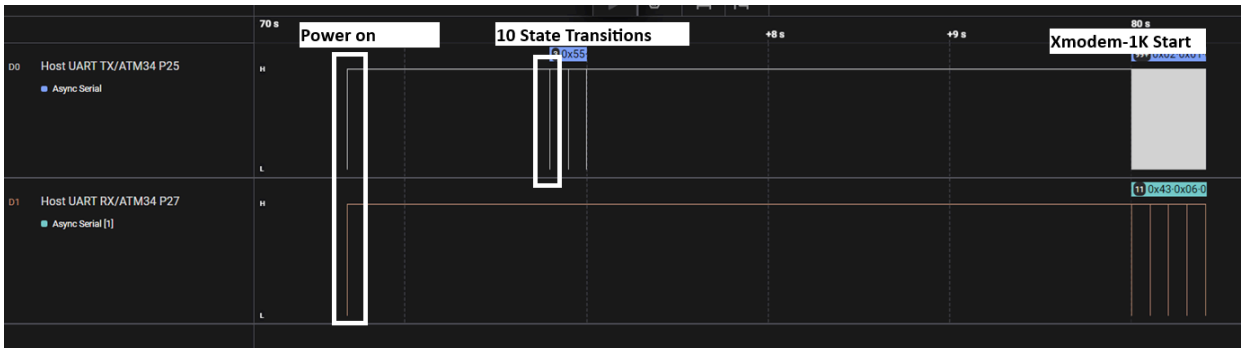

Figure 3-5 - Timing Diagram for Option #2 - Shared BBOOT (P25) and UART1 RX (P25)

This diagram differs slightly from Option#1 above. This diagram provides the Host UART TX and RX timing when the BBOOT and Host UART TX are shared on the same pin.

Revision History

Date	Version	Description
Nov. 25, 2025	0.50	Initial version created

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