ATM34/e ROM UART Bootloader

Application Note

SUMMARY: This document describes the ROM UART Bootloader feature for the ATM34/e Wireless SoC Series.

Atmosic™

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Acronyms and Abbreviations

Acronyms	Definition
ATM34/e	ATM3430e ATM3430 ATM3405
SoC	System-on-Chip

1. Overview

This document describes the ROM UART Bootloader feature and requirements for the ATM34/e Wireless SoC Series. This ROM UART Bootloader mode is intended to allow updating code into the ATM34's RRAM or Flash when the ATM34 device has never been programmed. ROM UART Bootloader mode is also applicable to the ATM34 devices that have been programmed. This feature enables the ATM34/e device to boot, load code into SRAM/RRAM/Flash, and continue executing code. The traditional way was to use SWD to program the device.

2. Hardware and Software Requirements

2.1 Supported EVKs

This document applies to:

EVK	SoC Package	SoC Part Number	Kit Part Number
Evaluation Kit for ATM3430e 7x7 QFN	56-pin 7x7 mm QFN	ATM3430E-5YCAQN	ATMEVK-3430e-YQN-5
Evaluation Kit for ATM3405 BGA	93-ball 4x4 mm BGA	ATM3405-5YCABV	ATMEVK-3405-YBV-5
Evaluation Kit for ATM3405 5x5 QFN	40-pin 5x5 mm QFN	ATM3405-5WCAQK ATM3405-5PCAQK	ATMEVK-3405-WQK-5

Table 2-1 - Supported ATM34/e Series EVKs

2.2 Supported Software

Please use the latest Atmosic OpenAir release at https://github.com/Atmosic/openair.

The ROM UART Bootloader tool package is available in Python scripts and Windows executables, and can be found at https://atmosic.com/software-utilities. For detailed usage, refer to the README.md files in the respective directories.

3.   ROM UART Bootloader Functionality

ROM UART Bootloader functionality allows a connected host over UART to download executable images using the Xmodem-1K protocol into ATM34's SRAM. The downloaded image loaded into the SRAM can, in turn, initiate the firmware download procedure with the attached host over UART to the RRAM or external/stacked Flash.

3.1   ROM UART Bootloader Theory of Operation

Mandatory Requirements for ATM34:
- VBAT/LI, and GND
- P25 (UART1 RX/BBOOT)
- P27 (UART1 TX)
- PWD (depending on operation)
- Host I/O level must match the ATM34 configured level. (i.e., I/O 1.8 V)

Upon powering on or asserting the PWD signal, ROM monitors the BBOOT (P25) state approximately at a minimum of 10 ms after. BBOOT assertion is an active high signal.
- If the BBOOT state is low, ROM continues the normal boot sequence
- If the ROM detects the BBOOT pin high, it monitors for 10 state transitions on P25 to activate the ROM UART Bootloader mode, as shown in the timing diagrams below
  - The host can initiate 10 state transitions by sending a character 'U' (Hex: 0x55) over the host UART TX (P25/UART1 RX/BBOOT)
  - Once activated, ATM34 ROM reconfigures BBOOT P25 as ATM34 UART1 RX and P27 as ATM34 UART1 TX. ROM sets the baud rate to 115200 bps, initiates Xmodem-1K protocol, and waits for the first Xmodem-1K protocol header from the host
  - The host can initiate Xmodem-1K data transfer to load code into SRAM for execution
  - Once the Xmodem-1K transfer is successful, the ROM starts executing code that was loaded into SRAM
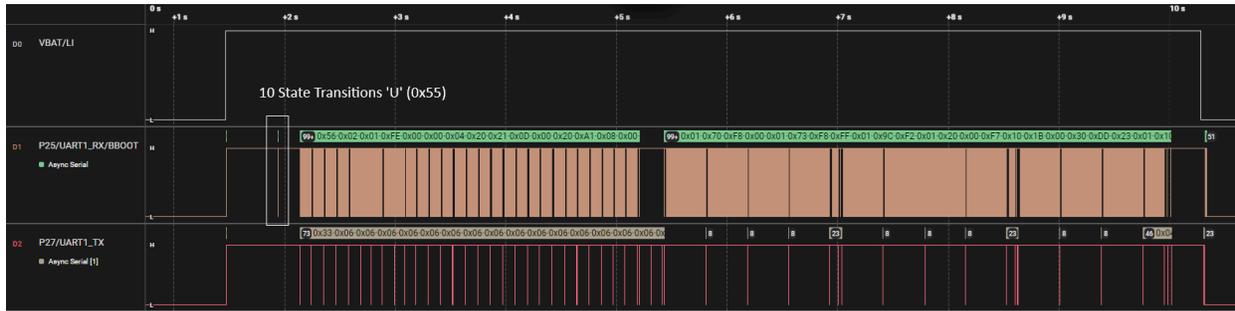
Figure 3-1 - Example of a Full ROM UART Bootloader Cycle Loading Image into RRAM
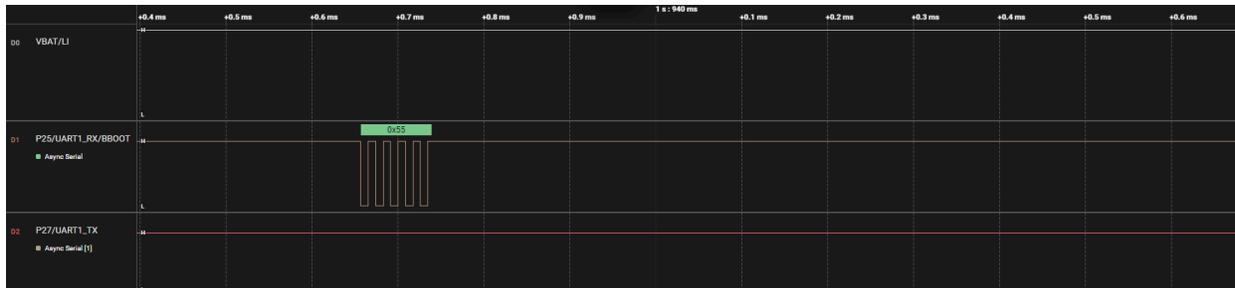
Figure 3-2 - Host P25 Transmitting 'U' (0x55) to initiate ROM UART Bootloader Mode

3.2   Security

ROM UART Bootloader feature can be disabled by programming OTP bit 56 (Refer to the atm_otp driver in the openair repository mentioned above). Once this bit is set, UART1 RX capability is disabled in hardware.

For recovery, the application and/or bootloader can unlock the ROM UART Bootloader functionality via a higher-layer authentication mechanism if needed.

4. ROM UART Bootloader Power-Up Sequence

The typical use of this ROM UART Bootloader feature is in manufacturing to load code into RRAM. Care must be taken when controlling the power-up sequence and control signals on the manufacturing test fixture to ensure proper operation. The following sections provide power-on and signal sequencing for specific cases.

- Recommended Power-On/PWD/Signal Sequencing
- Sequencing without PWD with the correct host P25 timing
- Sequencing with the incorrect host P25 timing

4.1 Recommended Power-On/PWD/Signal Sequencing

To ensure the ATM34 enters the correct ROM UART Bootloader mode, follow this specific timing sequence, and a timing example is shown below:

- Power Initialization: Apply power to the ATM34 first
- Reset (PWD) Control: Ensure the PWD signal is held at least 0.7 V for a minimum of 1 ms to guarantee a proper reset
- BBOOT Pin (P25) Setup: Once PWD is deasserted (released), the host shall drive the P25 pin HIGH
    - Recommend to assert P25 HIGH as soon as VBAT/LI is powered on and before PWD assertion
- The Sampling Window: This HIGH signal on P25 must be established within 10 ms of PWD deassertion. This is the critical window where the ROM samples the BBOOT pin to enter "monitoring mode"
    - Do not recommend asserting P25 HIGH close to the 10 ms mark. Capacitance can impact this timing. Enable as soon as possible
- Mode Entry: Once in monitoring mode, the ATM34 looks for 10 state transitions before entering the ROM UART Bootloader mode

Figure 4-1 - Example of a Full ROM UART Bootloader Cycle Loading Image into RRAM with PWD

Figure 4-2 - Example of the Recommended Power-On and Host Enabling Control Sequence with PWD

4.2 Sequencing Without PWD With the Correct Host P25 Timing

To ensure the ATM34 enters the correct ROM UART Bootloader mode, follow this specific timing sequence if the PWD can not be added to the manufacturing test fixture. A timing example is shown below:

- Power Initialization: Apply power to the ATM34 first
- BBOOT Pin (P25) Setup: Assert P25 HIGH as soon as VBAT/LI is powered on
- The Sampling Window: This HIGH signal on P25 must be established within 10 ms of when VBAT/LI is powered on. This is the critical window where the ROM samples the BBOOT pin to enter "monitoring mode"
    - Do not recommend asserting P25 HIGH close to the 10 ms mark. Capacitance can impact this timing. Enable as soon as possible
- Mode Entry: Once in monitoring mode, the ATM34 looks for 10 state transitions before entering the ROM UART Bootloader mode
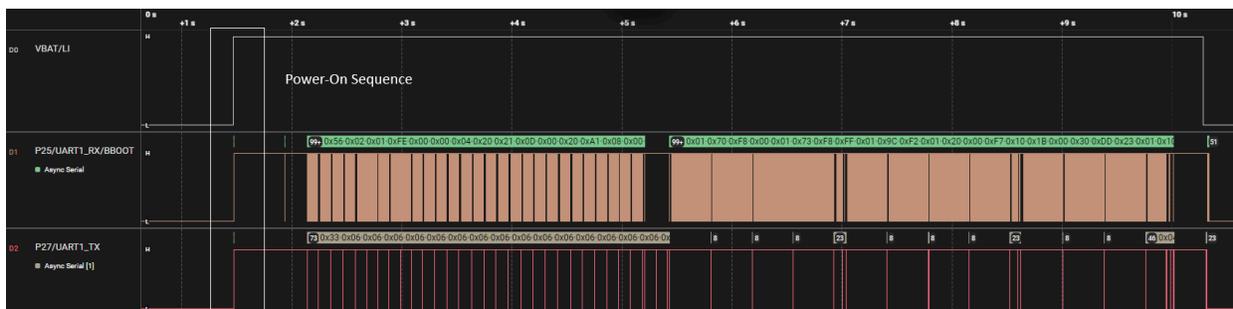

Figure 4-3 - Example of a Full ROM UART Bootloader Cycle Loading Image into RRAM Without PWD
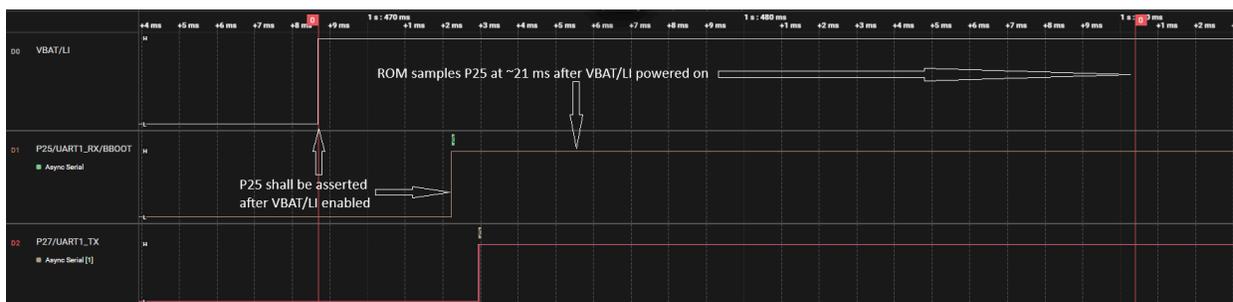

Figure 4-4 - Example of a Power-On and Host Enabling Control Sequence Without PWD

4.3   Sequencing With the Incorrect Host P25 Timing and PWD is Required

To ensure the ATM34 enters the correct ROM UART Bootloader mode, follow this specific timing sequence, and a timing example is shown below:

- Power Initialization: Apply power to the ATM34 first
- Reset (PWD) Control: Ensure the PWD signal is held at least 0.7 V for a minimum of 1 ms to guarantee a proper reset
- BBOOT Pin (P25) Setup: Once PWD is deasserted (released), the host shall drive the P25 pin HIGH
  - It is difficult for some setups to control P25 to start after VBAT/LI is powered on. This example requires PWD if P25 cannot be controlled to be driven after VBAT/LI. Powering up the ATM34 through its GPIO pins can cause the ATM34 to start in an incorrect state. Therefore, PWD is required to make sure ATM34 is reset to the default state
  - Recommend to assert P25 HIGH as soon as VBAT/LI is powered on and before PWD assertion
- The Sampling Window: This HIGH signal on P25 must be established within 10 ms of PWD deassertion. This is the critical window where the ROM samples the BBOOT pin to enter "monitoring mode"
  - Do not recommend asserting P25 HIGH close to the 10 ms mark. Capacitance can impact this timing. Enable as soon as possible
- Mode Entry: Once in monitoring mode, the ATM34 looks for 10 state transitions before entering the ROM UART Bootloader mode
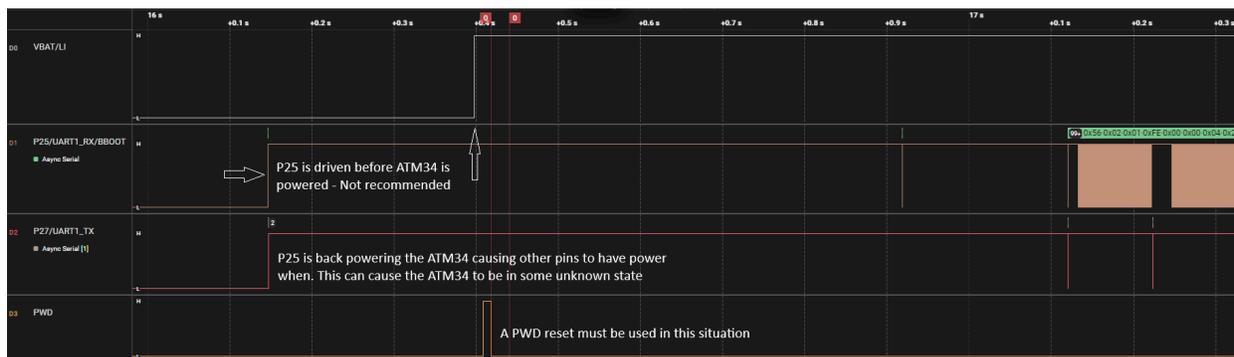

Figure 4-5 - Example of the Incorrect Power-On and Host Enabling Control Sequence with Added PWD

5. Example ROM UART Bootloader Feature With Functional Boot

This section provides an example of powering up and its signal sequencing to download a firmware image and then boot the downloaded firmware image. To ensure the ATM34 enters the correct ROM UART Bootloader mode and resets to the functional booting mode, follow this specific timing sequence. A timing example is shown below:

- Power Initialization: Apply power to the ATM34 first
- Reset (PWD) Control: Ensure the PWD signal is held at least 0.7 V for a minimum of 1 ms to guarantee a proper reset
- BBOOT Pin (P25) Setup: Once PWD is deasserted (released), the host shall drive the P25 pin HIGH
  - Recommend to assert P25 HIGH as soon as VBAT/LI is powered on and before PWD assertion
- The Sampling Window: This HIGH signal on P25 must be established within 10 ms of PWD deassertion. This is the critical window where the ROM samples the BBOOT pin to enter "monitoring mode"
  - Do not recommend asserting P25 HIGH close to the 10 ms mark. Capacitance can impact this timing. Enable as soon as possible
- Mode Entry: Once in monitoring mode, the ATM34 looks for 10 state transitions before entering the ROM UART Bootloader mode
- Functional Boot: Once the firmware image is downloaded into RRAM, powering off/on ATM34 or applying PWD without P25 asserted can start ATM34 into normal functioning boot mode

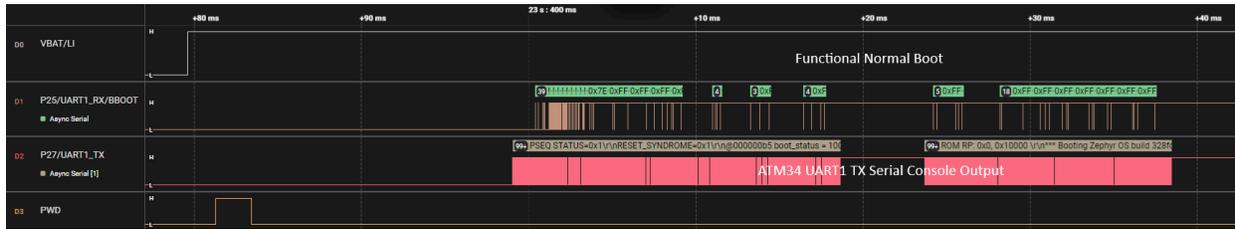*Figure 5-1 - Example of the Firmware Image Download with Functional Normal Boot*

Figure 5-2 - Zoomed-in of ATM34 Normal Boot with Serial Console Output

6. Additional Information

- Minimum 10 ms ROM sampling time depends on the capacitance of the different power rails. Using the Atmosic design capacitor values will result in approximately 21 ms when the Atmosic Wireless SoC exits out of a proper reset. The minimum time is 10 ms.   Atmosic does not recommend changing to different capacitor values in the Atmosic PMU-powered rails. Recommend to assert P25 as soon as VBAT/LI or PWD is enabled
- P25 being powered on before VBAT/LI is not recommended and should be avoided as much as possible
- If the power sequence can not be accurately controlled, then the PWD signal should be used to reset the ATM34 properly
- If a functional test is required after firmware download, ATM34 must be powered off/on, or PWD apply with P25 deasserted to run in functional normal operation mode
- A software retry mechanism should always be implemented if ATM34 does not respond due to power sequencing issues. This can be done by using software to control the power off/on of VBAT/LI, or asserting PWD after ATM34 failed to respond
- If cycling power, care should be taken to make sure capacitors are discharged; otherwise, a proper reset to the ATM34 might not be achieved

Revision History

Date	Version	Description
March 11, 2026	0.51	Update with more examples
Nov. 25, 2025	0.50	Initial version created

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