

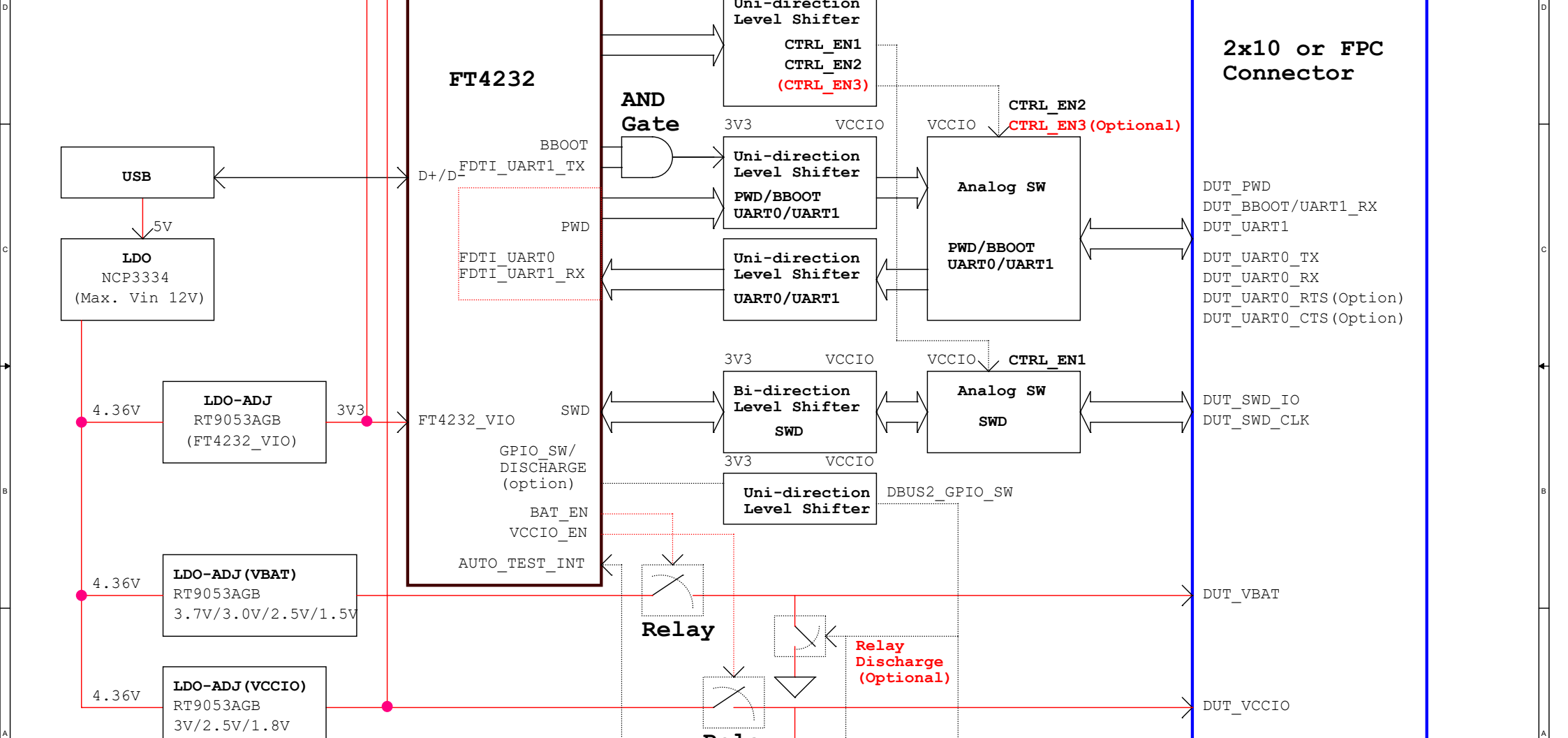
MP DOWNLOAD BOARD (DL)

Release Date	Revision	Design Eng.	Design Note
8/11/2020	Rev. 1	JOE	Initial release
8/20/2020	Rev. 2	JOE	1. Reduce Jump numbers 2. Add 1.8V VDDIO Jump
9/28/2020	Rev. 3	JOE	1. Replace the unidirection level shift U12 for BBOOT and PWD 2. Change VBAT and VCCIO 3.3V option to 3V. R17 and R20 change to 0ohm
10/26/2021	Rev. 4	JOE	1. Switching regulator U4 change from PWM mode to hysteresis mode, R18 connect to ground. 2. Add a GPIO1 control option from U1-pin24 (ADB4) to J1 2x10 connector pin17 3. Add S1 button to reset DUT
03/07/2022	Rev. 5	JOE	1. Add power control circuits for BAT/VCCIO/LS. 2. R43, R47, R51, R52, R53, R54, R57, R62, R122 change from 0 ohm to 62 ohm.
05/02/2022	Rev. 6	JOE	1. R43, R47, R51, R52, R53, R54, R57, R62, R122 change to 62 ohm. 2. Add FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8, FB9
02/24/2026	Rev. 7	JOE	1. Add photorelays and analog switches to enable connect/disconnect control of DUT VBAT, VCCIO, and control interfaces. 2. DUT VBAT voltage support: add 1.5V and 3.7V. 3. Add GPIO test functionality. 4. Add an 14 pin FPC connector to support atmosic reference design board. 5. Support GPIO interrupt-based trigger to start MPTool automated testing. 6. Y1-12MH crystal: Connect pins 2 and 4 from Not Connected (NC) to Ground.
04/07/2026	Rev. 7a	JOE	1. Replace the unidirection level shifter from NL3V4T244MU2AG-Q to TXU0104DTR. 2. Connect a 1 kohm resistor R333 in series between pin 15 of U34 and PWD_RESET_DUT. 3. Change the connection between SWCLK_DUT and R272 from pin 10 to pin 9 of the CN1 FPC connector.

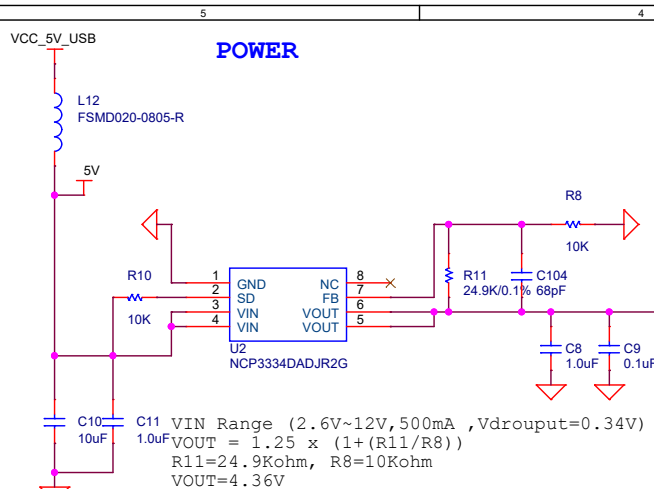
Atmosic Technologies, Inc

ATMOSIC TECHNOLOGIES INC			
Title		Atmosic MP Download Board - TITLE	
Size B	Document Number	Rev 7a	
Date:		Wednesday, April 08, 2026	Sheet 1 of 10

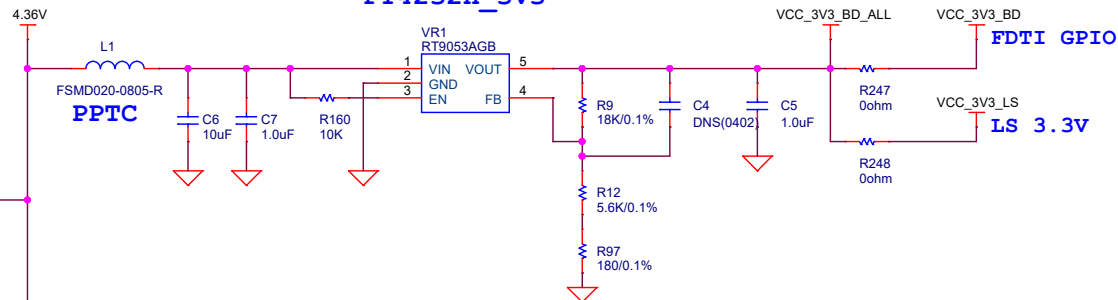
5	4	3	2	1
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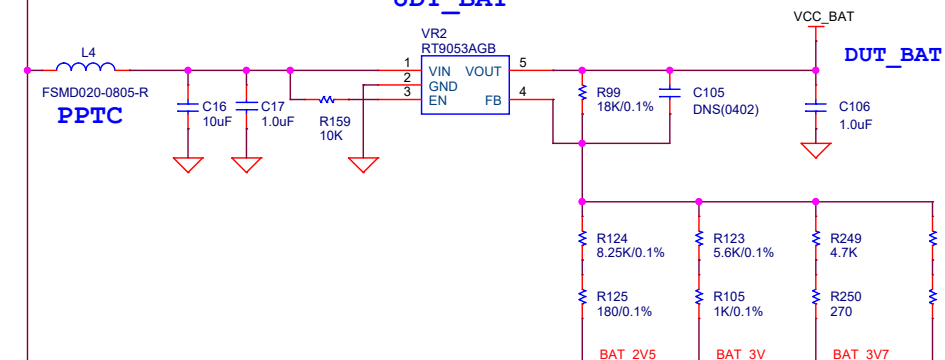
POWER



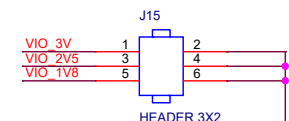
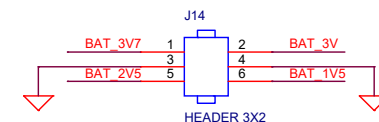
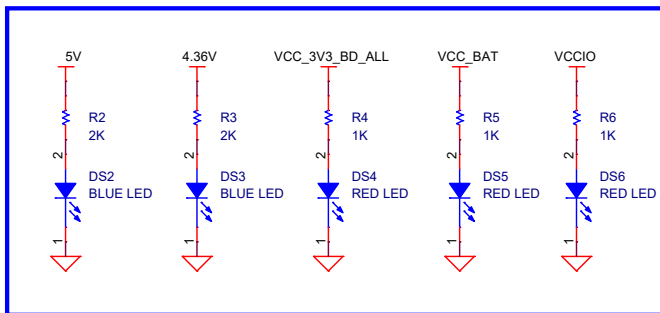
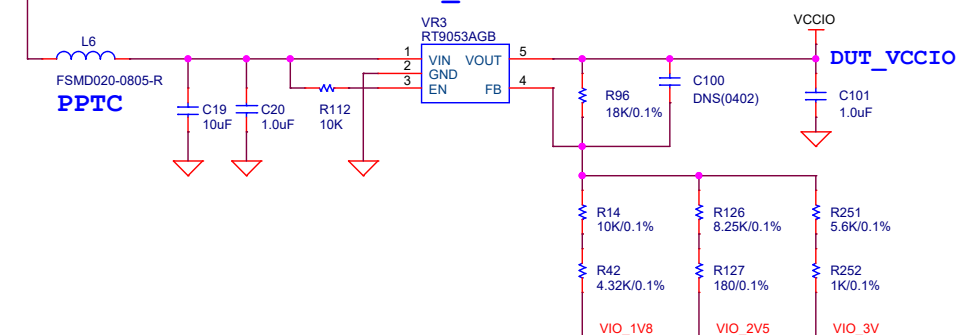
FT4232H_3V3



UDT_BAT



DUT_VDDIO



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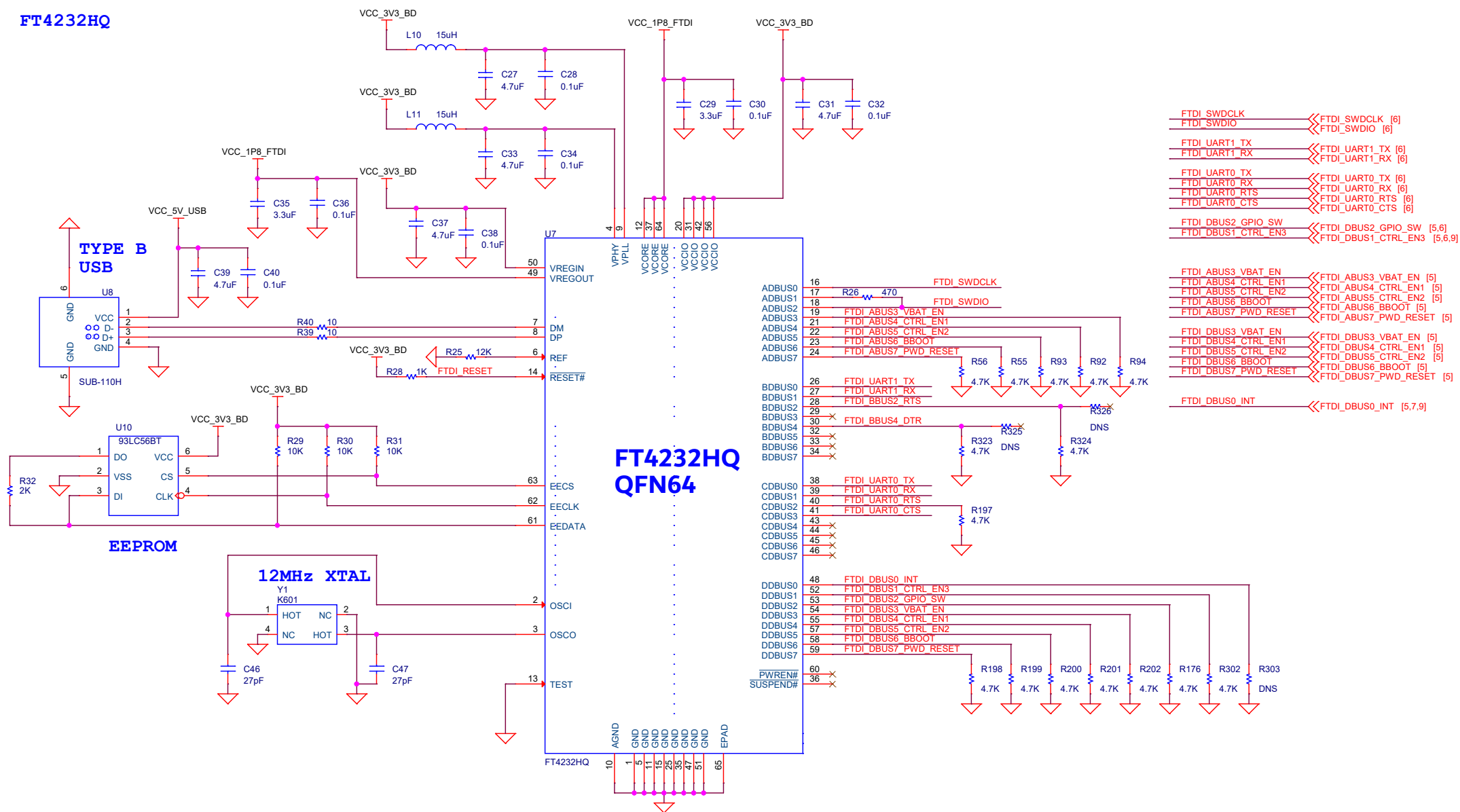
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Size B Document Number <Doc>

Rev 7a

Date: Wednesday, April 08, 2026 Sheet 3 of 10

FT4232HQ



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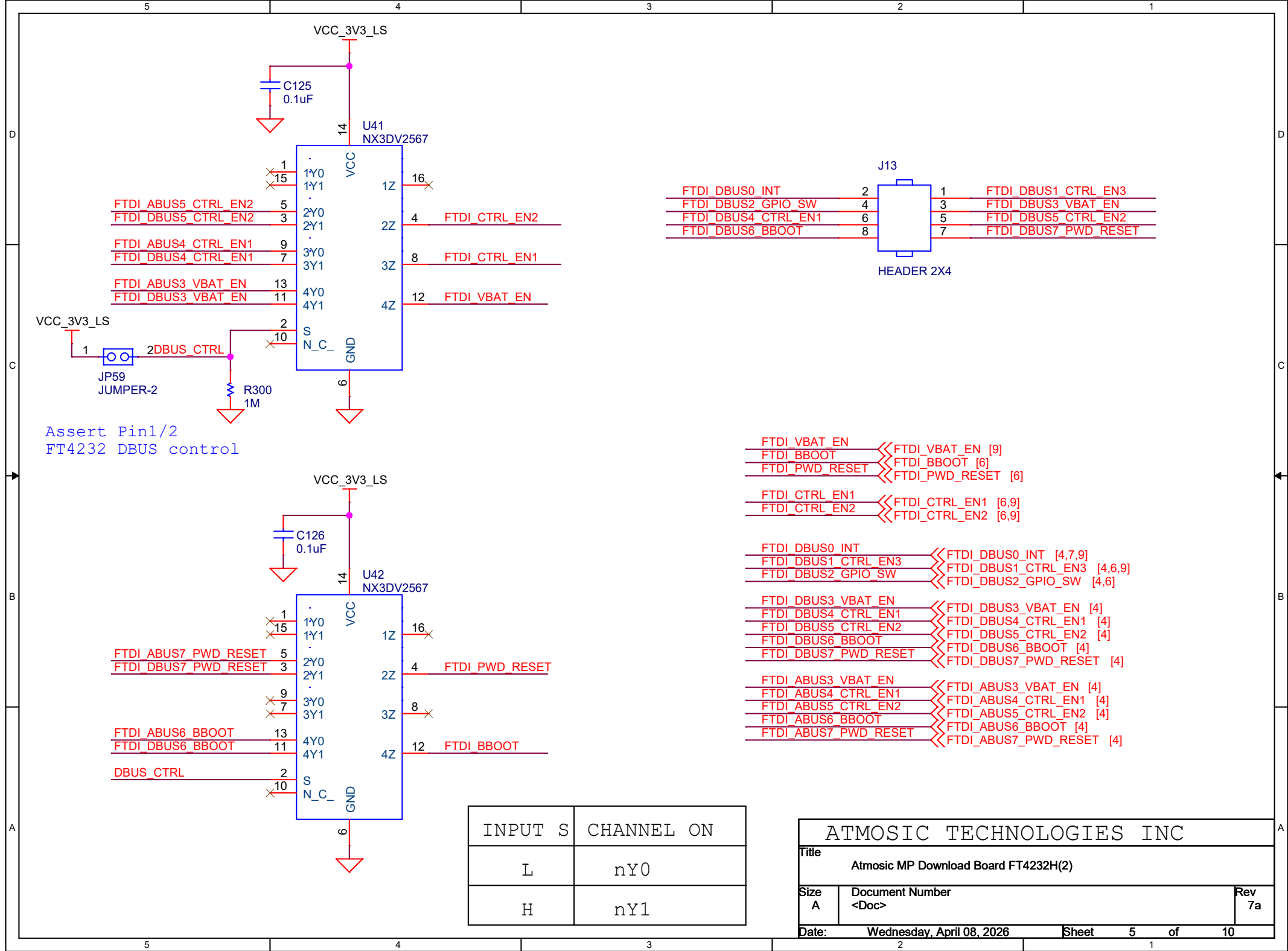
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Size B	Document Number <Doc>
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Rev	7a
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Date: Wednesday, April 08, 2026

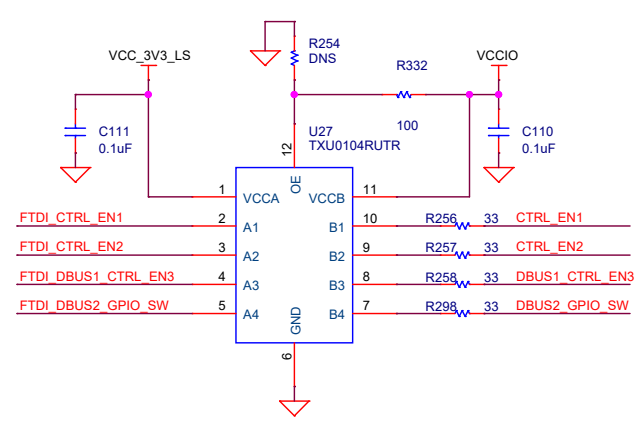
Sheet 4 of 10



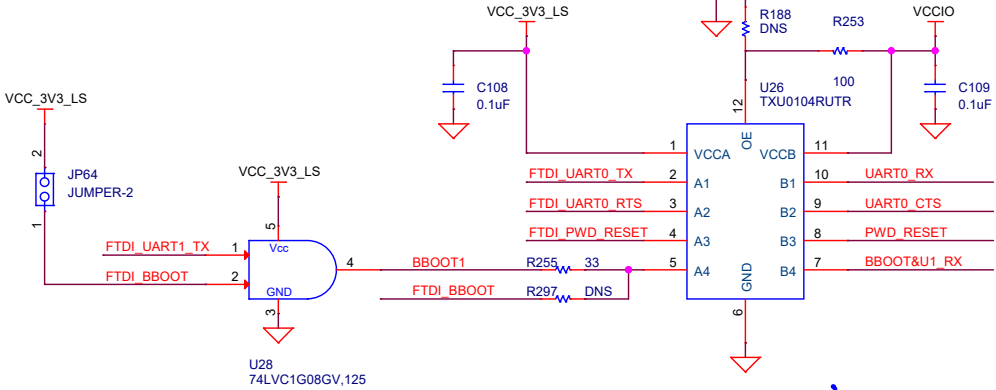
INPUT S	CHANNEL ON
L	nY0
H	nY1

ATMOSIC TECHNOLOGIES INC		
Title Atmosic MP Download Board FT4232H(2)		
Size A	Document Number <Doc>	Rev 7a
Date:	Wednesday, April 08, 2026	Sheet 5 of 10

LEVEL_SHIFTER



Uni-direction Level Shifter



74LVC1G08GV,125 (AND) Uni-direction Level Shifter

PIN1 (FTDI_BBOOT)	PIN2 (FTDI_UART1_TX)	PIN4 (OUT)	SUPPORT MODE
H	H	H	BBOOT and ROM_UART
L	H	L	NORMAL

Note: Add a jumper to JP64 to manually pull high FTDI_BBOOT signal and then enable the UART1 bootloader firmware download function.

- FTDI_CTRL_EN1 <-> FTDI_CTRL_EN1 [5,9]
- FTDI_CTRL_EN2 <-> FTDI_CTRL_EN2 [5,9]
- FTDI_DBUS1_CTRL_EN3 <-> FTDI_DBUS1_CTRL_EN3 [4,5,9]
- FTDI_DBUS2_GPIO_SW <-> FTDI_DBUS2_GPIO_SW [4,5]

- FTDI_BBOOT <-> FTDI_BBOOT [5]
- FTDI_PWD_RESET <-> FTDI_PWD_RESET [5]

- FTDI_SWCLK <-> FTDI_SWCLK [4]
- FTDI_SWDIO <-> FTDI_SWDIO [4]

- FTDI_UART1_TX <-> FTDI_UART1_TX [4]
- FTDI_UART1_RX <-> FTDI_UART1_RX [4]

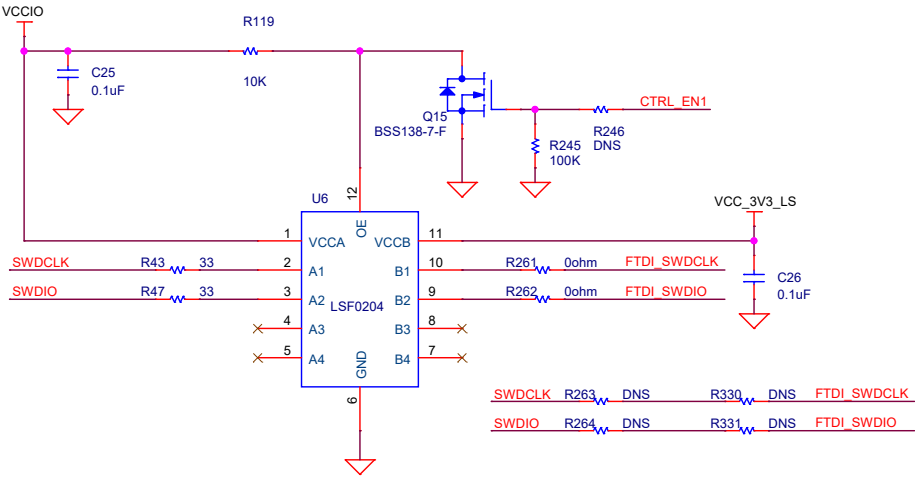
- FTDI_UART0_TX <-> FTDI_UART0_TX [4]
- FTDI_UART0_RX <-> FTDI_UART0_RX [4]
- FTDI_UART0_RTS <-> FTDI_UART0_RTS [4]
- FTDI_UART0_CTS <-> FTDI_UART0_CTS [4]

- CTRL_EN1 <-> CTRL_EN1 [7]
- CTRL_EN2 <-> CTRL_EN2 [7]
- DBUS1_CTRL_EN3 <-> DBUS1_CTRL_EN3 [7]
- DBUS2_GPIO_SW <-> DBUS2_GPIO_SW [8,10]

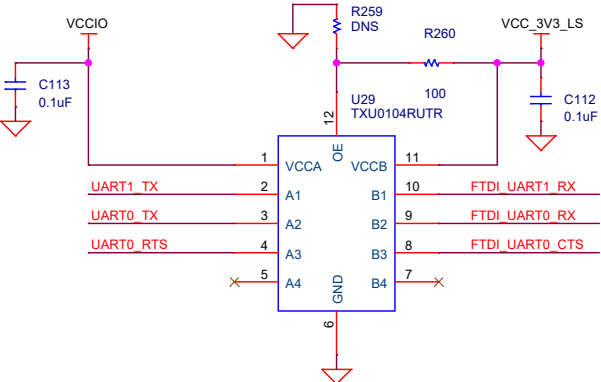
- BBOOT&U1_RX <-> BBOOT&U1_RX [7]
- PWD_RESET <-> PWD_RESET [7]

- SWCLK <-> SWCLK [7]
- SWDIO <-> SWDIO [7]
- UART1_TX <-> UART1_TX [7]

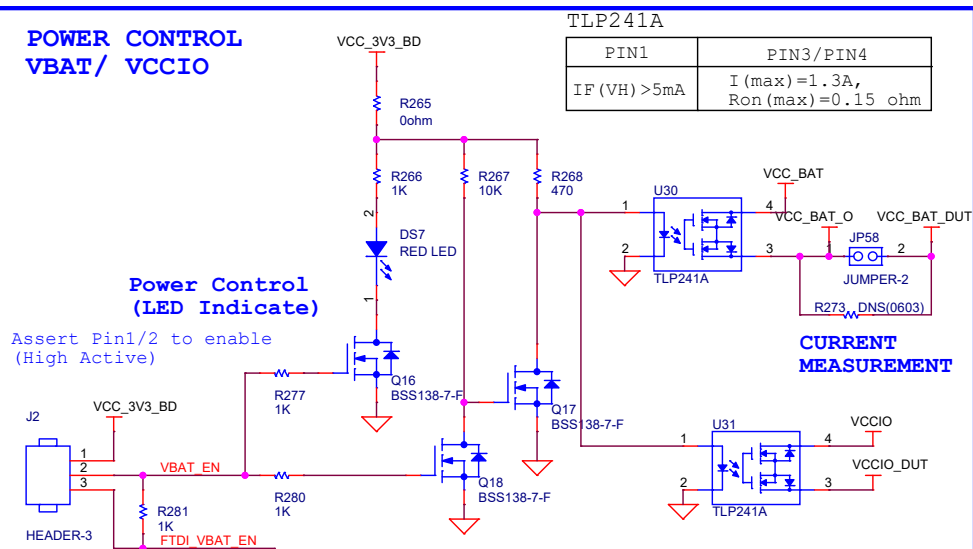
- UART0_TX <-> UART0_TX [7]
- UART0_RX <-> UART0_RX [7]
- UART0_RTS <-> UART0_RTS [7]
- UART0_CTS <-> UART0_CTS [7]



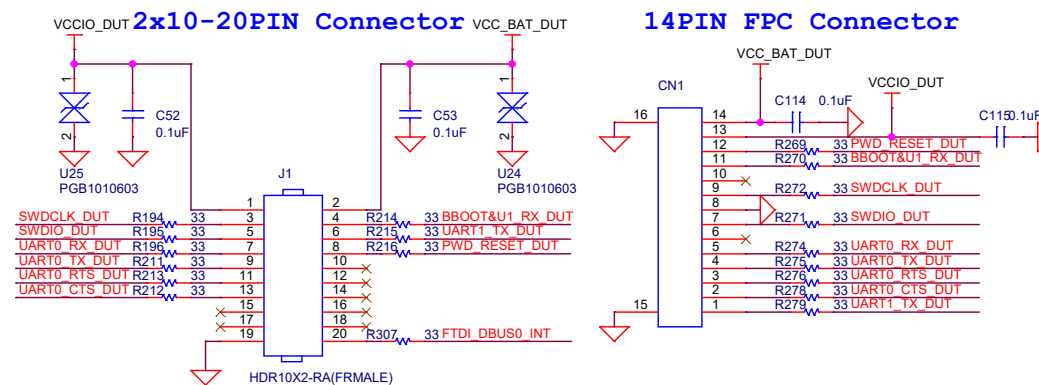
Bi-direction Level Shifter



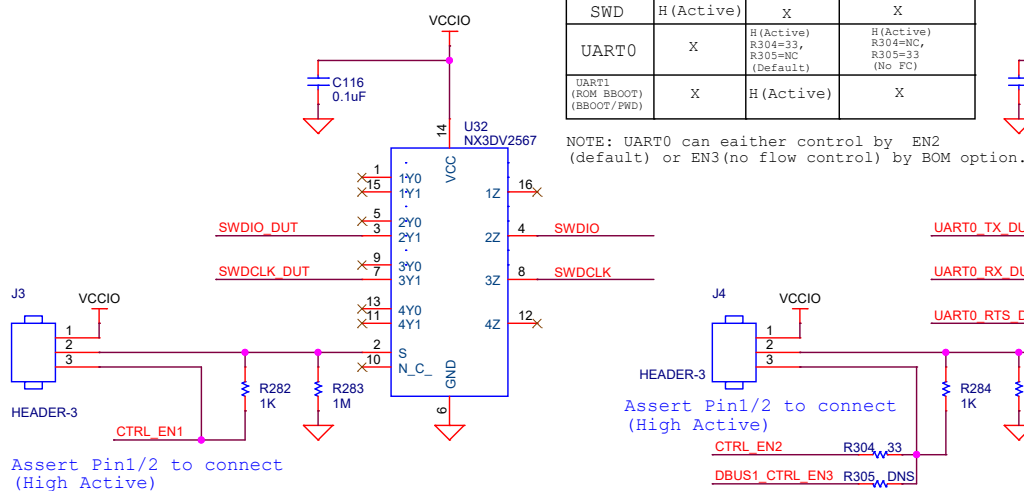
Uni-direction Level Shifter

POWER CONTROL
VBAT/ VCCIO

INTERFACE



SIGNAL CONNECT/DISCONNECT SWITCH
DUT SWD/UART0/UART1



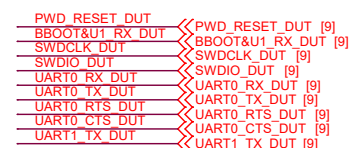
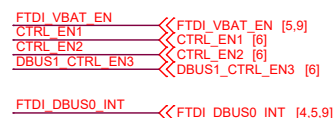
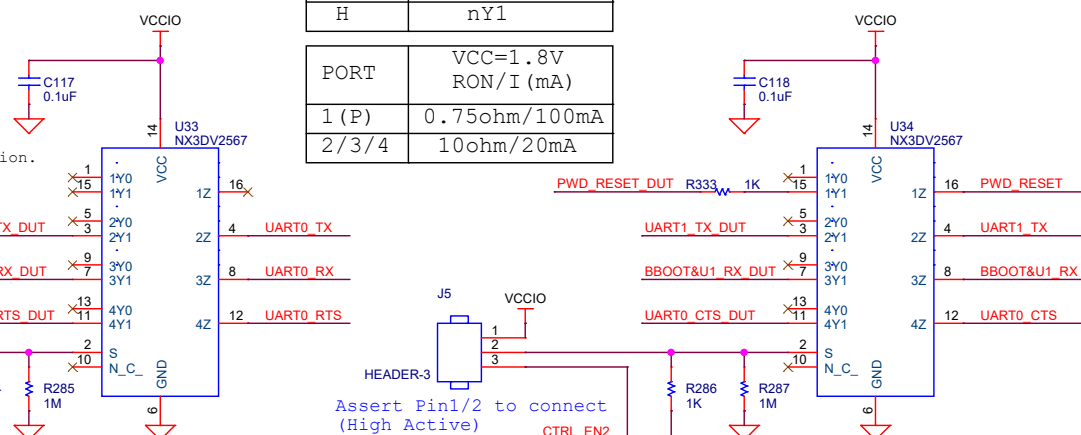
CTRL	EN1	EN2	EN3 (Option)
SWD	H (Active)	X	X
UART0	X	H (Active) R304=33, R305=NC (Default)	H (Active) R304=NC, R305=33 (No FC)
UART1 (ROM BOOT) (BOOT/PWD)	X	H (Active)	X

NOTE: UART0 can either control by EN2 (default) or EN3(no flow control) by BOM option.

NX3DV2567

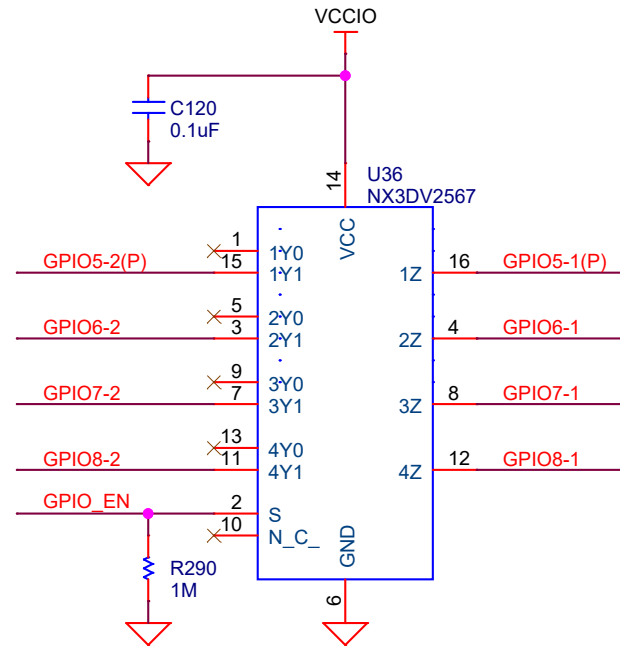
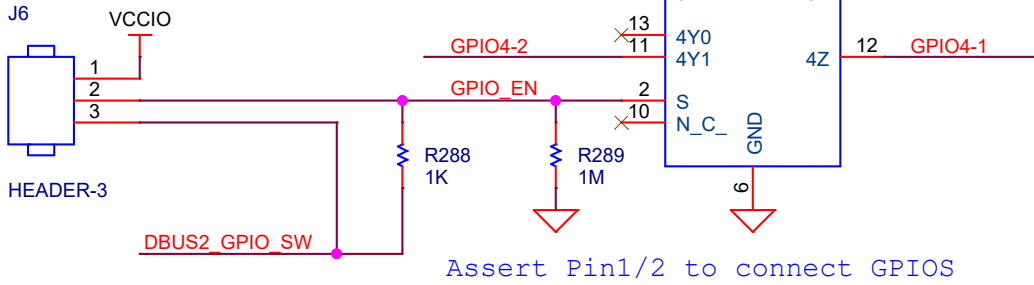
IN_S	CHANNEL ON
L	nY0
H	nY1

PORT	VCC=1.8V RON/I (mA)
1 (P)	0.75ohm/100mA
2/3/4	10ohm/20mA



GPIO TEST

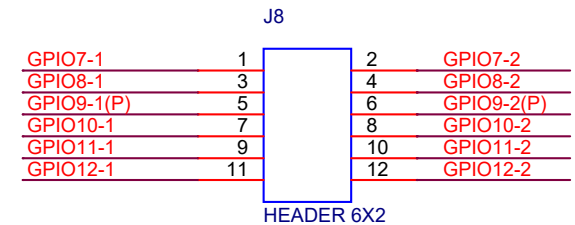
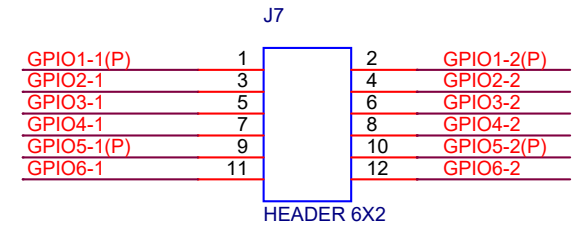
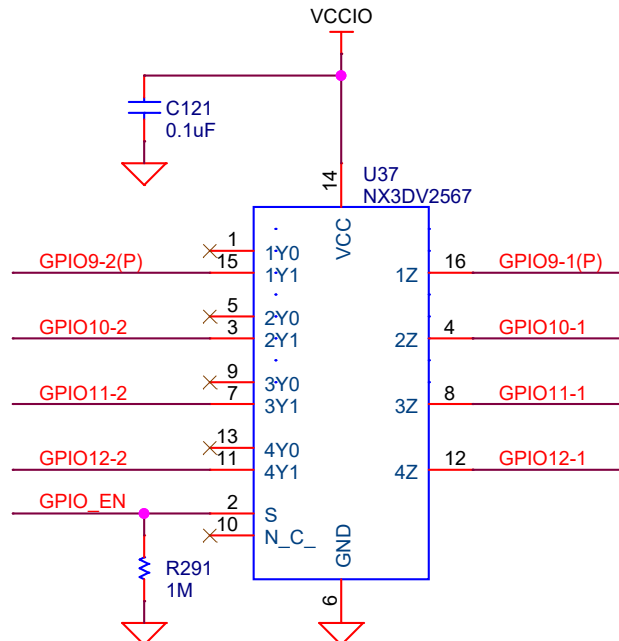
Install PIN1/2 to
conntec GPIO
(High Active)



DBUS2_GPIO_SW <<DBUS2_GPIO_SW [6,10]

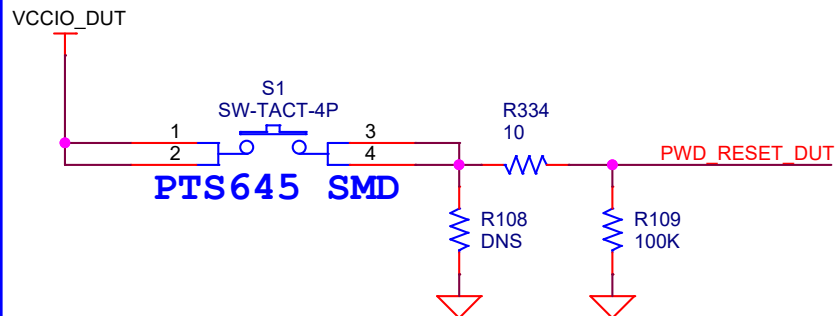
INPUT S	CHANNEL ON
L	nY0
H	nY1

PORT	VCC=1.8V RON/I (mA)
1 (P)	0.75ohm/100mA
2/3/4	10ohm/20mA

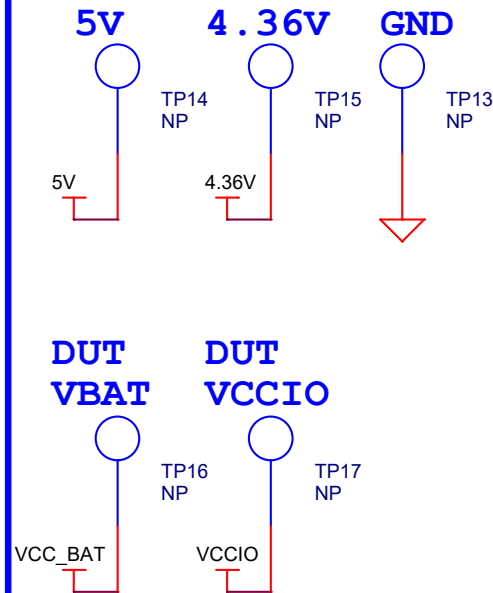


ATMOSIC TECHNOLOGIES INC		
Title Atmosic MP Download Board - GPIO TEST		
Size A	Document Number <Doc>	Rev 7a
Date:	Wednesday, April 08, 2026	Sheet 8 of 10

RESET



POWER

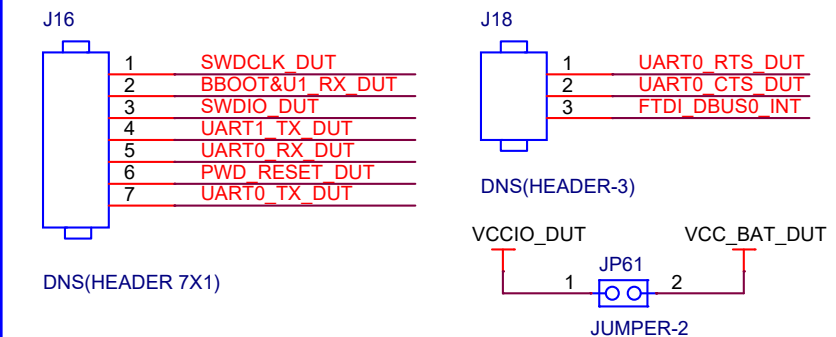


PWD RESET DUT << PWD_RESET_DUT [7]
 BBOOT&U1_RX_DUT << BBOOT&U1_RX_DUT [7]
 SWDCLK_DUT << SWDCLK_DUT [7]
 SWDIO_DUT << SWDIO_DUT [7]
 UART0_RX_DUT << UART0_RX_DUT [7]
 UART0_TX_DUT << UART0_TX_DUT [7]
 UART0_RTS_DUT << UART0_RTS_DUT [7]
 UART0_CTS_DUT << UART0_CTS_DUT [7]
 UART1_TX_DUT << UART1_TX_DUT [7]

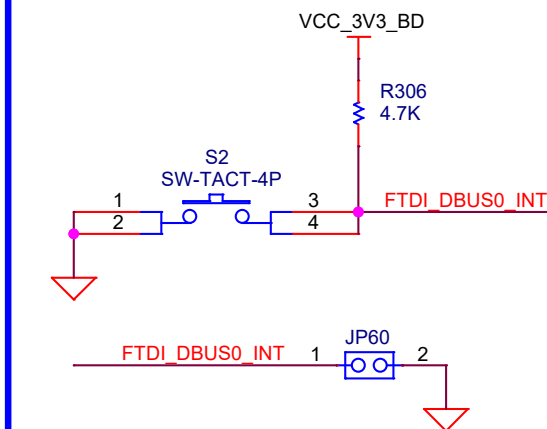
FTDI_VBAT_EN << FTDI_VBAT_EN [5]
 FTDI_CTRL_EN1 << FTDI_CTRL_EN1 [5,6]
 FTDI_CTRL_EN2 << FTDI_CTRL_EN2 [5,6]
 FTDI_DBUS1_CTRL_EN3 << FTDI_DBUS1_CTRL_EN3 [4,5,6]

FTDI_DBUS0_INT << FTDI_DBUS0_INT [4,5,7]

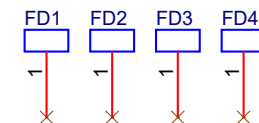
TEST POINT-DUT



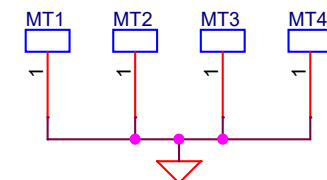
AUTO TEST



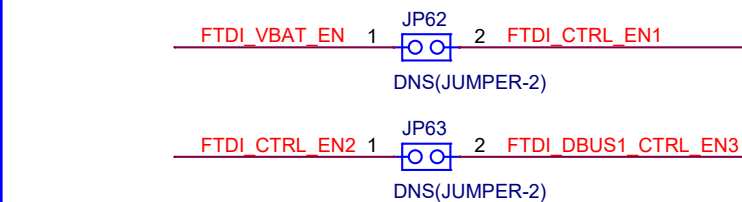
BOARD FIDUCIALS



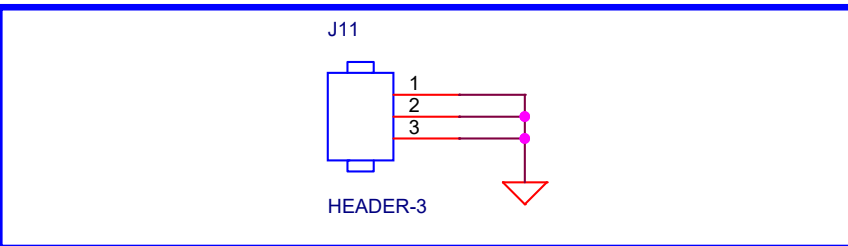
MOUNTING HOLES



TEST POINT- CONTROL



GND

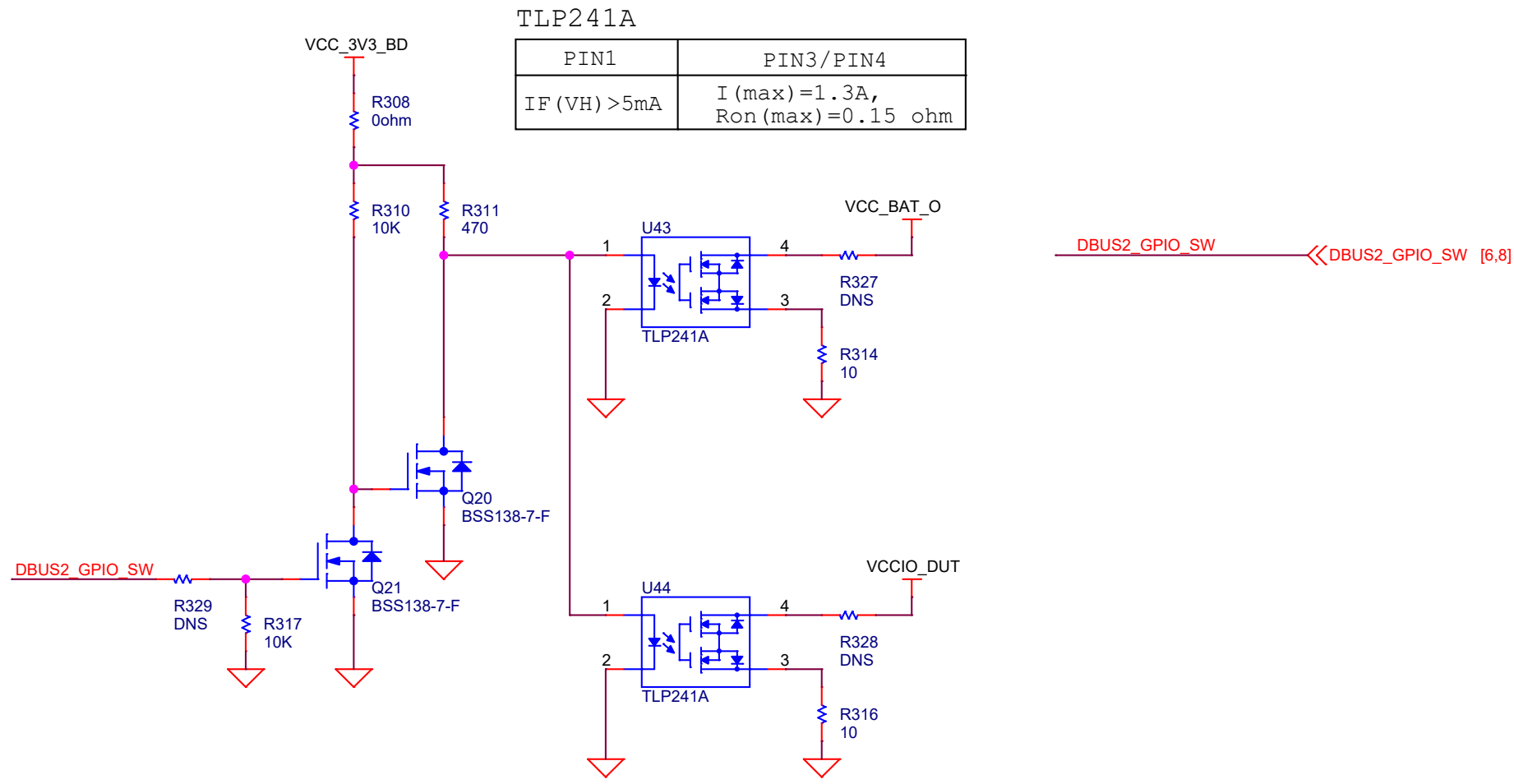


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Title		
Atmosic MP Download Board - RESET/ AUTO TEST/ TEST PINS		
Size	Document Number	Rev
A	<Doc>	7a
Date:	Wednesday, April 08, 2026	Sheet 9 of 10

5 4 3 2 1

D
C
B
A



TLP241A

PIN1	PIN3/PIN4
I F (VH) >5mA	I (max)=1.3A, Ron (max)=0.15 ohm