Overview

The ATM5/e Wireless SoC Series is a member of extreme low-power Bluetooth® system-on-chip (SoC) solutions. This Bluetooth Low Energy SoC Series integrates a Bluetooth 6.3/5.4 compliant radio with ARM® Cortex® M33F application processor, 256 KB Random Access Memory (RAM), 512 KB Read Only Memory (ROM), up to 2048KB nonvolatile memory (NVM), with ARM® TrustZone® enabled security features, and state-of-the-art power management to enable maximum lifetime in battery-operated devices.

The ATM5/e Series includes two subseries:

- **ATM53/e subseries**: Full-featured (Bluetooth 6.3, including Channel Sounding and Inline PCT Transfer)
- **ATM52/e subseries**: Bluetooth 5.4 (no Channel Sounding)

The extremely low power ATM5/e Series SoC, with 2.0 mA active receiving and 3.1 mA active transmitting power consumption, is designed to extend battery life for the Internet-of-Things (IoT) markets. Support for low duty cycle operation allows systems to run for significantly longer periods without changing or recharging the battery. In addition, the ATM5305e SoC supports operation from energy harvesting sources such as photovoltaic.

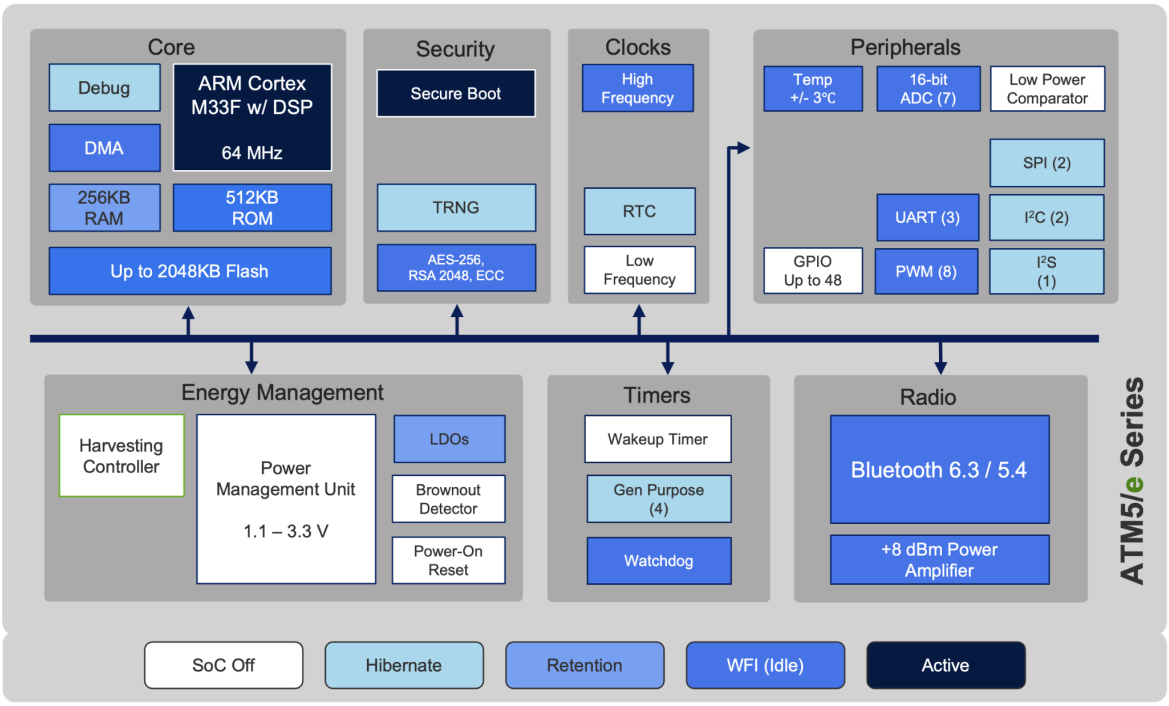
Applications

Enterprise Segment

- Asset Tracking
- Logistical Management
- Industrial IoT Sensors
- Remote Monitoring
- Medical Equipment Tracking
- Patient and Staff tracking

Consumer Segment

- Personal Asset Tracker
- Embedded Tag and Tracker
- Environmental Control
- Advanced Home Automation
- Consumer IoT
- Patient Health Monitor



Features

Bluetooth 6.3/5.4

- Bluetooth Low Energy
- 2 Mbps, 1 Mbps, 500 kbps, and 125 kbps PHY rates
- Bluetooth 6.3 Channel Sounding, including Inline PCT Transfer **(ATM53/e only)**

MCU and Memory

- 64 MHz ARM® Cortex® M33F MCU
- 512 KB ROM, 256 KB RAM, 1 MB or 2 MB NVM
- Retention RAM configuration: 16 KB to 256 KB in 16 KB step sizes
- 32 MHz / Optional 32.768 kHz Crystal Oscillator

Security

- ARM® TrustZone®, HW Root of Trust, Secure Boot, Secure Execution & Debug
- AES-128/256, SHA-2/HMAC 256 Encryption/Cryptographic Hardware Accelerators
- True random number generator (TRNG)

Energy Harvesting (ATM5305e only)

- Harvesting Controller Supports photovoltaic energy source

RF and Power Management

- Fully integrated RF front-end
- Maximum Tx Output Power: +8 dBm
- 1.1 to 1.6V†† or 1.7 to 3.3V battery input voltage with integrated Power Management Unit (PMU)
- Active power consumption with a 3 V battery, includes SoC and Radio power consumption
  - Rx @ -95 dBm: 2.0 mA**
  - Tx @ 0 dBm: 3.1 mA**
- SoC typical power consumption with a 3 V battery, including PMU
  - Retention @ 128KB RAM: 2.0 µA**
  - Retention @ 256KB RAM: 2.4 µA**
  - Hibernate: 1.1 µA**
  - SoC Off: 300 nA**

Interfaces

- I^2C, I^2S, SPI, UART, PWM, GPIO
- 16-bit ADC

Package Options

Product	Package (GPIOs)	Bluetooth Standard	Channel Sounding	Energy Harvesting
ATM5305e	5x5 mm 40-pin QFN (24)	6.3	✓	✓
ATM5305	5x5 mm 40-pin QFN (24) 4x4 mm 94-ball BGA (48)	6.3	✓	N/A
ATM5205	5x5 mm 40-pin QFN (24) 4x4 mm 94-ball BGA (48)	5.4	N/A	N/A

RTOS and Development Tool

- Supports open source Zephyr RTOS, including SDK, Toolchain, as well as Visual Studio Code IDE

Feature Highlights

The ATM5/e Series SoC has designed-in features that make it the best solution for a **low power Bluetooth Low-Energy product**. ATM53e Family SoC has a dedicated harvesting controller to boost and monitor energy from photovoltaic energy source.

The **integrated Power Management Unit (PMU)** is extremely efficient at providing the core and I/O power for the SoC, eliminating the need for an external PMU.

The Bluetooth Core supports advanced applications, including **Bluetooth 6.3 Channel Sounding** applications with Inline PCT Transfer (ATM53/e only).

ATM5/e Series comprehensive set of **Peripherals** includes multiple UARTs, I2C masters, general-purpose SPI masters, multiple Pulse Width Modulation (PWM) outputs, Analog Comparators, and a 7-channel 16-bit ADC. The number of peripherals supported is based on pin muxing configuration.

†† will be available and validated at later time

** to be finalized after characterization

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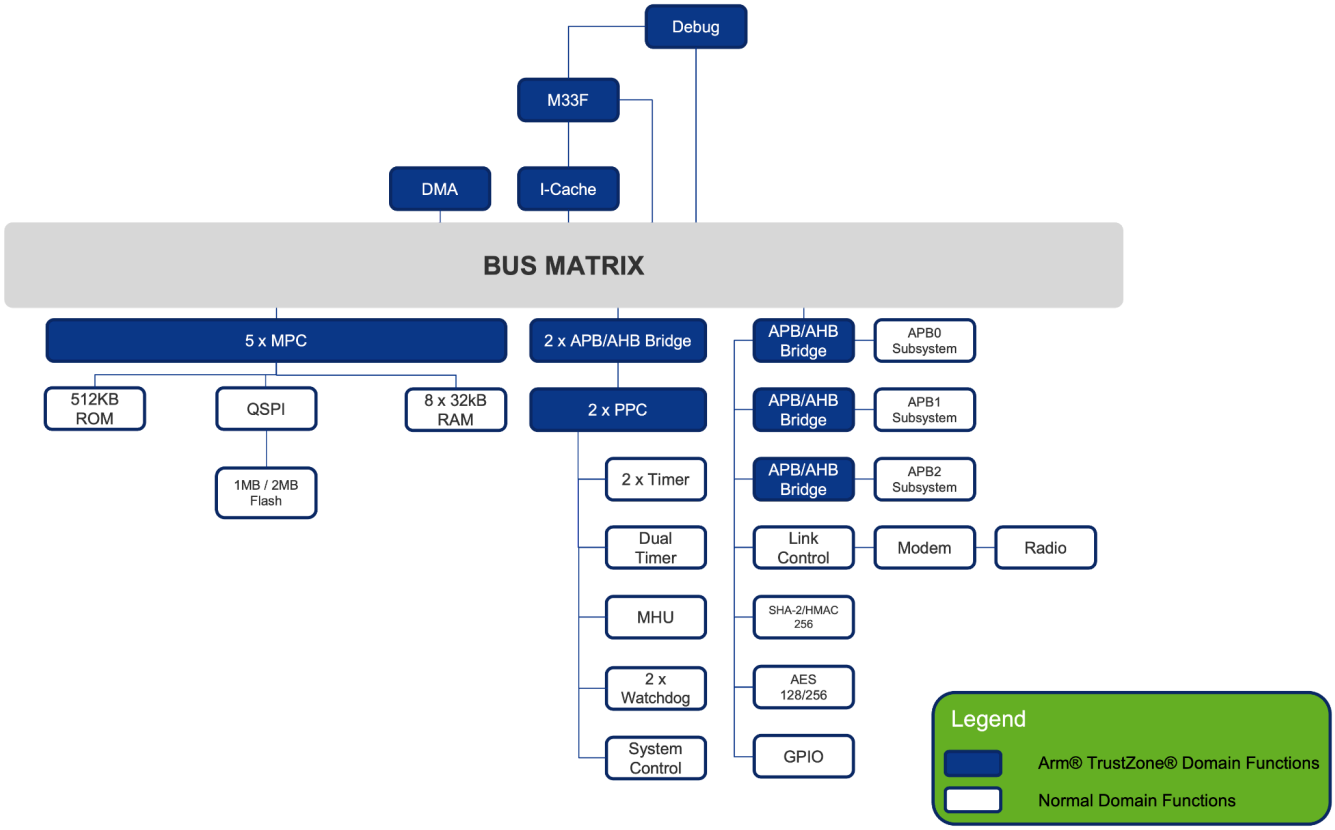
1 Functional Description

Figure 1-1 Functional Block Diagram



1.1 MCU & Memory

The ATM5/e contains a 64 MHz 32-bit ARM® Cortex®-M33F processor that is optimized for low-power operation. The processor is a little-endian, 32-bit RISC processor which implements the ARMv8-M architecture specification. It supports all Thumb-1/Thumb-2 instructions. It features four breakpoints, a serial access debug port, 117 interrupts, a single cycle multiplier, full wake-on-interrupt support, and two watchpoints. The M33F includes an IEEE-754-compliant floating point unit (FPU). The M33F also supports ARMv8-M Digital Signal Processing (DSP) extension for audio and sensor applications. The M33F core is configured with a 2 KB instruction cache to minimize instruction fetch latency.

To reduce latency, the software can use the Direct Memory Access (DMA) core for memory-to-memory copying and for initializing blocks of memory to a constant. When it is in use, the DMA core masters the Advanced Microcontroller Bus Architecture (AMBA) High-performance Bus (AHB) and has higher precedence than the Cortex®-M33F. When interfacing with different slaves, the DMA and MCU can operate concurrently.

The ATM5/e includes the following memory components:

- ROM: 512 KB of ROM. Core elements of the firmware are placed in ROM to add security, as well as extend application space and reduce latency.
- SRAM: The ATM5/e provides 256 KB of SRAM containing both system RAM and data RAM organized as sixteen 16 KB macros. The power state of each macro in each low-power state can be independently controlled.
- NVM: The ATM5/e is designed to provide a scalable NVM option. The ATM5/e offers 2048 KB or 1024 KB of non-volatile memory (NVM) to store configuration, calibration data, and user application code and data.

Table 1.1-1 System Memory Map

Start	Stop	Block
0x0000 0000	0x0008 FFFF	ROM + NVM [Non-secure]
0x1000 0000	0x1008 FFFF	ROM + NVM (secure]
0x0020 0000	0x002F FFFF	Extended NVM [Non-secure]
0x1020 0000	0x102F FFFF	Extended NVM [Secure]
0X2000 0000	0x2003 FFFF	SRAM [Non-secure]
0x3000 0000	0x3003 FFFF	SRAM [Secure]
0x4000 0000	0x4030 4FFF	Timers, Watchdogs, GPIO, UART, PWM, SPI, I^2C, OTP, PMU, PSEQ, GADC, Sensor Hub, I^2S, DMA, SHA-2/HMAC 256 and AES-128/256 [Non-secure]
0x5000 0000	0x5030 4FFF	All of the above peripherals are aliased in secure space [Secure]

Non-secure and Secure address aliases are used by the Cortex processor in secure or non-secure mode. The physical mapping of the resource (memory, peripherals) to that alias is managed by the Memory Protection Controller (MPC) and Peripheral Protection Controller (PPC). Please refer to the ***Arm® TrustZone Technology for the Arm v8-M Architecture*** manual.

1.1.1 Clocks

Primary clock domains in the ATM5/e are:

- Low-power clock: 32.768 kHz crystal or an internal RC oscillator (RCOSC) for low-power operations
- RF clock: 8 MHz and 16 MHz fixed frequency clocks used by the link controller, modem, and radio subsystem
- Backplane clock: 32, 48, or 64 MHz backplane clock used by the MCU and peripherals
- I^2S: 16, 24, 32, 48, or 64 MHz for internal core operation
- Peripheral: 16MHz fixed frequency clock used by certain peripherals

The Real Time Counter (RTC) is a free-running counter running off of the Low-power clock. It is accessible by the MCU for timestamping and only restarts when the SoC undergoes a cold start.

1.1.2 Reset

The Power Management Unit (PMU) releases the chip-wide reset once the power supplies have stabilized, which allows the SoC to cold start. There is no explicit reset pin, but the power-down (PWD) pin can be used to power cycle the ATM5/e. The MCU can reset individual peripherals and the SoC via control registers.

1.1.3 Power Modes

The ATM5/e supports five primary power states, which are Active, Retention, Hibernation, SoC Off, and Powerdown. Each primary state may have several secondary states depending on the number of active power domains and clock gating. All power states except Powerdown are managed by the power sequencer block (PSEQ).

1. **Active**: All regions of the ATM5/e are powered on. Active power can be optimized by clock gating peripherals and/or entering these secondary states:
    - Radio Deep Sleep: The RF clock is gated while the remainder of the ATM5/e is active.
    - MCU Idle: MCU executes the Wait for Interrupt (WFI) instruction to gate internal clocks.

2. **Retention**: All or some of the 256 KB SRAM can be retained in increments of 16 KB. All register/flip-flop states needed to resume operation after waking up are retained. Digital I/Os will not lose state during Retention. The ATM5/e supports many wakeup options including a timer expiring, activity detected on GPIO's, debug activity over SWD, and the analog comparator.

3. **Hibernation**: Powers down system memory. A minimal number of registers/flip-flops remain powered on. Digital I/Os will not lose state during Hibernation. The ATM5/e supports many wakeup options, including a timer expiring, activity detected on GPIOs, debug activity over SWD, and the analog comparator. The MCU undergoes a reboot when waking from this state.

4. **SoC Off**: All digital domains, including the top-level digital domain and RTC, are powered off, but the PMU remains in an ultra-low-power state with limited functionality. The SoC undergoes a cold start when waking from this state. Wake mechanisms are limited to:

    - special 40-bit timer
    - high-level input on P39/SOCOFF_WAKE
    - ultra-low power analog comparator with input on either P37 or P38.

5. **Powerdown** (PWD pin asserted): All power domains, including the PMU, are completely shut off. No supplies are internally generated or maintained.

1.2 Communications Radio

1.2.1 Radio

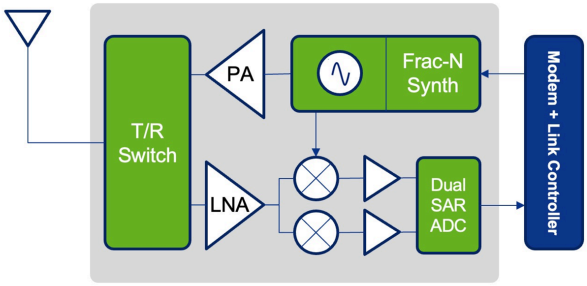
The 2.4GHz radio, shown in Figure 1.2-1, is designed to support extremely low power operation for Bluetooth Low Energy communication standards.

The radio is a single-ended shared RF interface that is internally split for receive and transmit radio communication chains.

- The receive chain includes the LNA, downconversion, mixer, IF amplifier, anti-aliasing filter, and two successive approximation analog-to-digital converters (ADC). The anti-aliasing filter, LNA, and IF amplifier are controlled by the AGC to maximize performance across the dynamic range.

- The transmit chain uses the digital direct frequency modulation of a fractional-N synthesizer to create the appropriate signal that is amplified by a power amplifier to provide the desired RF output level.

Figure 1.2-1 Radio Block Diagram



1.2.2 Modem

The modem, along with the radio, link controller, and software stack, forms a highly efficient Bluetooth Low Energy solution.

The Bluetooth Low Energy radio supports the 2 Mbps high-speed PHY, the 1 Mbps basic PHY, and the 500 kbps and 125 kbps Coded-PHY. The basic 1 Mbps PHY is fully compatible with Bluetooth 4.0 specifications, while the newer 2 Mbps rate can provide 2X the speed. For long-range, the Coded-PHY can provide up to 4X range. The radio architecture is also optimized for burst data transmission using Frequency-Hopping Spread Spectrum (FHSS) over 40 channels with 2 MHz spacing (3 advertising channels/37 data channels). For Channel Sounding, the modem and radio support the 1 Mbps, 2 Mbps, and 2Mbps with BT of 2.0 PHYs.

During receive operation, the modem and radio are enabled prior to expected packet reception as determined by the link controller. Incoming packets are detected, tracked, processed, and forwarded to the link controller. The modem and radio receiver are turned off by the link controller at the end of a completed packet. Channel information is provided directly from the link controller to the radio without the involvement of the modem.

There is minimal involvement of the modem during transmission activity. The link controller provides the symbol bit stream, which is then shaped consistent with the signal requirements to provide the appropriate frequency deviation by the radio. Channel information and target transmit power are provided directly from the link controller to the radio.

1.2.3 Link Controller (ATLC)

The Atmosic Link Controller (ATLC) provides an interface between the MCU, modem, and tightly-coupled memory (TCM), allowing the MCU to access through the system AHB bus to the control registers and tightly coupled memory.

During transmission, the software writes the packet payload and control structures into the TCM. The link controller serializes the data into a bit stream to the modem.

During receive, the operation is reversed. Received data from the modem is processed and stored in the TCM and read by software.

The design runs on an 8 MHz clock and is synchronous to the modem (16 MHz), AHB bus (16 MHz), and TCM (16 MHz).

1.3 Power Management Unit (PMU)

The Power Management Unit (PMU) provides the core and I/O power supplies to the ATM5/e. The PMU on ATM5305e has a dedicated harvesting controller to boost and monitor energy from external photovoltaic energy sources. The PMU generates DVDD, VDDIO, and VBAT3V or VBAT1V depending on how the MODE pin is tied, which itself depends on the voltage of the power source used. For more information on the board connections, refer to the *ATM5/e Hardware Design Guide*.

The PMU provides brownout interrupts to enable more reliable operation.

Table 1.3-1 PMU External Pins

Pin	Description
MODE	● Tie to VBAT3V to select VBAT3V input connection for a 3V battery, or ● Tie to ground for VBAT1V to be connected to a 1V battery.
VBAT3V (BUCK MODE Input)	BUCK MODE (tied to VBAT3V): 3 V Battery input, input range is 1.7 V to 3.3 V BOOST MODE (tied to ground): PMU to generate 1.9-3.3V
VBAT1V (BOOST MODE Input)	BUCK MODE: PMU to generate 1.15 V supply (Tx Power < 8dBm) or 1.30V (Tx Power = 8dBm) BOOST MODE: 1V Battery input
VDDPA	Power supply input for the transmit power amplifier BUCK MODE : Tie to VBAT1V BOOST MODE: Tie to VDDIO
MON_VSTORE (ATM5305e only)	Higher voltage measurement pin, designed for up to 4.5 V Input only.
DVDD	DVDD is sourced internally from VBAT1V, and is the digital supply pin. This pin needs to only be tied to a bypass capacitor.
VBAT1V_A	VBAT1V_A is sourced from VBAT1V, and is the radio input supply pin.
VDDIO	VDDIO is a PMU-generated 1.8 V I/O supply output
SW	PMU switching node. Must be connected to VBAT1V through an inductor.

1.3.1 PMU Configurations

The PMU must be configured correctly to ensure correct operation. The following modes of operation are supported by the PMU:

Table 1.3.1-1 PMU Configuration

PMU Configuration	MODE Connection	VBAT3V Connection	VBAT1V Connection	VDDIO Connection
Battery or external power supply (1.8 V-3.3 V) with internally generated I/O supply	VBAT3V	Battery or power supply	Inductor from SW to VBAT1V	VDDIO
Battery or external power supply (1.1 V-1.5 V) with internally generated I/O supply	Ground	10 µF bypass capacitor	Battery or power supply	VDDIO

1.4 Security

The ATM5/e offers a complete security solution, including:

- Secure boot
- Secure OTA
- Secure execution
- Key management
- Key storage
- Secure debugging

The ATM5/e has a true random number generator (TRNG), which generates a single 32-bit random number per invocation. Arbitrarily long random numbers can be achieved by repeatedly invoking this random number generator. The TRNG can also be used to seed a software hash function.

The ATM5/e also has two hardware cryptographic accelerators, AES-128/256 and SHA-2/HMAC 256, which are both accessible by software. There are provisions to load keys into the AES-128/256 where the keys themselves are not readable by any bus master.

1.5 OTP Access

The 512-byte one-time programmable memory (OTP) is used to store PMU, security, and Radio configurations. The MCU can access the OTP via a controller that provides indirect access for byte reads and bit writes.

1.6 Timers and Interrupts

1.6.1 Wakeup Timer

The wakeup timer is a 40-bit timer based on the Low-power clock. When this timer is enabled during SoC Off mode, it will determine the SoC Off duration.

1.6.2 General Purpose Timers

There are four (4) general-purpose timer cores: Timer0, Timer1, Dual Timer, and Slow Timer. The values of the timers are readable by the MCU. Timer0, Timer1, and Dual Timer are clocked by the Peripheral clock, while the Slow Timer is clocked by the Low-power clock. All of these timers stop when the system enters a low-power state.

- Timer0 will decrement from a 32-bit load value and trigger a maskable interrupt as it transitions from 1 to 0. The reload value is loaded as the next timer value when the timer reaches 0. Additionally, there is a prescaler in front of each timer that can reduce the incoming clock by factors of 2 up to 256.
- Timer1 is identical to Timer0 with its own register space and its own interrupt.
- Dual Timer contains two timers that are independent from each other but trigger a shared maskable interrupt as either transitions from 1 to 0. Each timer counts down and can run in one-shot, periodic, or free-running mode. The timers are configurable to be either 16-bit or 32-bit. Additionally, there is a prescaler in front of each timer that can reduce the incoming clock by factors of 2 up to 256.
- Slow Timer is a 40-bit countdown timer with three programmable thresholds. Maskable interrupts are optionally asserted when the counter counts from threshold + 1 to the threshold and from 1 to 0.

1.6.3 Interrupts

The ATM5/e supports the following categories of interrupts:

- Interrupts for ARM MCU exceptions, watchdog timers, and hardware protection blocks.
- Other maskable interrupts:
  - 26 interrupts for APB peripherals
  - 4 DMA interrupts
  - 4 primary communications radio interrupts
  - 11 timer and clocking interrupts
  - 50 GPIO interrupts (93-ball BGA, 4x4mm), 23 GPIO interrupts (40-pin QFN, 5x5mm)

1.7 Peripherals and I/O

The following peripherals are supported by the ATM5/e:

- **GPIO**
  There are up to 48 GPIOs available in the 93-ball BGA 4x4mm package, and 24 GPIOs in the 40-pin QFN 5x5mm package. GPIOs are controlled through software-accessible registers. In addition to drive, sample, pull-up, and pull-down functions, the GPIOs can also be used to generate interrupts and to wake the ATM5/e from low-power states.
- **I^2C**
  There are two identical I^2C master cores in which the software preloads the transaction and then initiates the hardware controller. Software can either poll for completion or respond to the completion interrupt. The I^2C clock is programmable to specific frequencies between 3.9 kHz and 2 MHz and supports clock stretching.
- **Serial Peripheral Interface (SPI)**
  The ATM5/e implements two identical SPI master cores with DMA support. The software can preload the transaction, initiate it, and then either poll for completion or respond to the completion interrupt. Opcode, transaction type, data, and number of bytes are all software programmable. The hardware will serialize and sample incoming data as required by the protocol. The SPI port clock frequency is programmable to specific rates between 7.8 kHz and 8 MHz.
- **UART**
  The ATM5/e implements three UART cores with flow control and DMA support. UART0 is typically used as a 4-wire host controller interface (HCI), while UART1 is typically used as a 2-wire debug interface. The baud rate is programmable to specific values between 16 to 2000000.
- **I^2S**
  The I^2S master core is designed to support an inter-IC sound bus for transporting digital audio data streams. This interface consists of:
  - SCK - system clock, bit clock, or serial clock
  - WS - word select, frame clock, or left/right clock
  - SD - serial data or data line

Depending on how the core is configured, the module sources or sinks these interface signals. Supported operation modes are PCM mode, left-justified mode, and right-justified mode.

- **PWM**
  The PWM has eight independent pulse width modulation output channels. Each channel can operate in one of four modes:
  1. Continuous mode - The user specifies the duty cycle and the PWM channel outputs.
  2. Counting mode - The user specifies the number of times to repeat in addition to the duty cycle. This combination of duty cycle and repeat count is referred to as a frame.
  3. IR mode - The PWM channel outputs one frame type and, immediately on completion of the first frame, outputs a second frame. This second frame can be identical to the first, or it can be different if a different set of parameters were loaded in while the first frame was going out.
  4. IR FIFO mode - The PWM core pulls the next frame information from a FIFO. One FIFO buffer is time-shared among all eight channels; therefore, IR FIFO mode is only supported in the channel equipped with the FIFO buffer.

  All channels support all modes of operation.

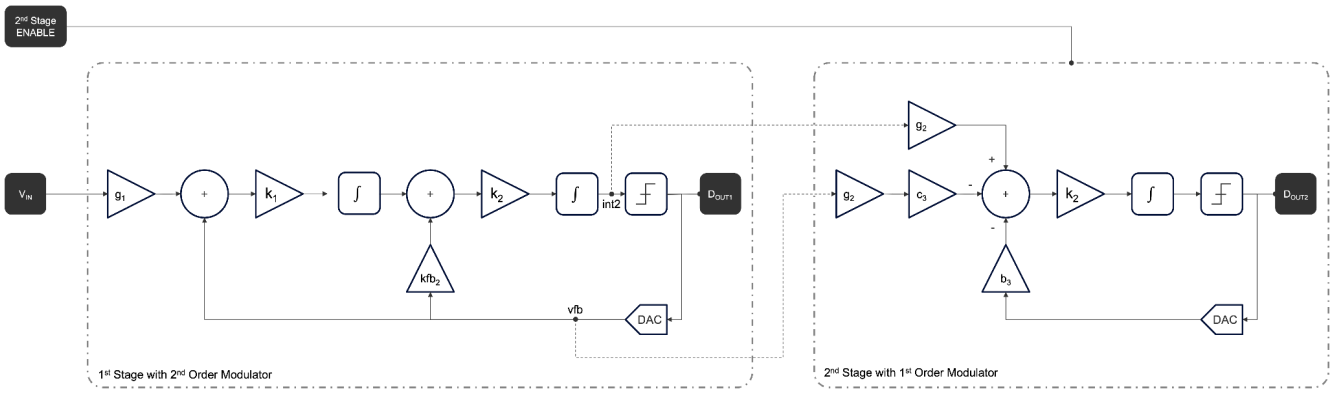
  PWM frequency ranges from 122 Hz to 8 MHz with 16-bit fields to independently control high duration and low duration.

- **Analog Comparator**
  The analog comparator provides an ultra-low power approach to sense an analog input signal from sensors and can optionally wake up the ATM5/e from a low-power state. The threshold level is programmable to one of 16 values between 150 mV and 1.65 V.

- **Application ADC**
  The General-purpose 16-bit Analog-to-Digital Converter (GADC) has a MASH 2-1 Sigma-Delta architecture, as shown in Figure 1.7-1. The 1st and 2nd Stages generate D_{out1} and D_{out2} bit streams, respectively, which are post-processed in the digital core to provide 16-bit output samples that are stored in a FIFO for software access. The GADC supports 11 physical input channels: VBAT, MON_VSTORE, AVDD1, internal temperature sensor, P37, P38, P39, P40, P41, P42, and P43.

For the maximum number of general-purpose peripherals supported in each package (GADC, UART, SPI, I^2S, I^2C, PWM), please refer to Part Ordering.

Figure 1.7-1 General Analog-to-Digital Converter (GADC) Architecture



1.8 Pin Multiplexing

The 48 programmable I/O pins of the 4x4 mm 93-ball BGA package may be programmed and connected to multiple functional signals, and the 5x5 mm 40-pin QFN package supports 24 programmable pins.

In addition, each of these I/O pins can be configured to enable an internal pull-up or pull-down as well as one of 4 drive strength levels. A pin multiplexing tool provided in the SDK can be used to program the I/Os to the desired function.

2 Electrical Specification

All parameters' typical values are based on a 3 V supply at 25 °C unless otherwise specified, and if specified, min/max values are based on the worst-case process variation, voltage, and ambient temperature conditions. Radio parameters are measured using a conducted configuration.

Table 2-1 Maximum Electrical Ratings[1]

Symbol	Parameter	Min	Typ	Max	Unit
VBAT3V	Battery supply			3.6	V
VBAT1V	Battery voltage	-0.2		1.7	V
VDDPA	PA supply	-0.2		3.6	V
VDDIO	I/O supply	-0.2		3.6	V
VBAT1V_A	Analog and Radio supply	-0.2		1.7	V
DVDD	Digital supply	-0.2		1.7	V
MON_VSTORE	High Voltage monitor pin (> 3.6 V)	-0.2		4.5	V
VIO	I/O pin (VDDIO > 3.4 V)	-0.2		3.6	V
VRF	RF I/O pin as input			10	dBm
ESD_{HBM}	ESD HBM			2000	V
ESD_{CDM}	ESD CDM			500	V
T_{STORE}	Storage Temperature	-40		125	°C

[1] Maximum ratings represent the highest levels to which the chip can be exposed for a short duration without incurring permanent damage. Prolonged exposure to these absolute maximum ratings may compromise the reliability of the device.

Table 2-2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDDIO	I/O supply	1.7	1.8	3.3	V
VBAT3V	Battery supply	1.7	3.0	3.3	V
VBAT1V	Battery supply	1.1	1.5	1.6	V
VDDPA	PA supply	1.7	1.8	1.9	V
VBAT1V_A	Analog and Radio Supply	0.95	1.1	1.4	V
DVDD	PMU Auxiliary Supply	0.8	1.1	1.4	V
VIO	I/O pin	0		VDDIO+0.2	V
	Crystal (Tolerance + Stability) - 32.000 MHz	-50		50	ppm
	Crystal (Tolerance + Stability) - 32.768 kHz	-500		500	ppm
TA	Operating (Ambient) Temperature	-40	25	85	°C

Table 2-3 Radio Transceiver Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Frequency		2.402		2.480	GHz
Rx sensitivity	37-byte packets, clean Tx				
	125 kbps		-101		dBm
	500 kbps		-98		dBm
	1 Mbps		-95		dBm
	2 Mbps		-90		dBm
	255-byte packets, dirty Tx				
	125 kbps		-99		dBm
	500 kbps		-96		dBm
	1 Mbps		-93		dBm
	2 Mbps		-90		dBm

Parameter	Conditions	Min	Typ	Max	Unit
Rx Carrier-to-Interferer	1 Mbps, Co-channel 1 Mbps, Adjacent 1 MHz 1 Mbps, Adjacent 2 MHz 1 Mbps, Adjacent 3 MHz		15 3 -35 -40	21 15 -17 -27	dB dB dB dB
Tx output power		-20		8	dBm
Tx power accuracy			+/-1.5		dB
Tx spectral mask	1 Mbps, 2 MHz offset 1 Mbps, > 3 MHz offset			-20 -30	dBm dBm
RSSI resolution			1		dB
RSSI accuracy	-90 to -20 dBm		+/-2		dB

Table 2-4 PMU Characteristics[2]

Parameter	Conditions	Min	Typ	Max	Unit
VBAT1V Output Voltage (with battery supply at VBAT3V)		0.95	1.1	1.4	V
VBAT3V Output Voltage (with battery supply at VBAT1V)		1.7	2.85	3.3	V
VDDIO Output Voltage		1.71	1.8	1.89	V

Table 2-5 GPIO Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Input VIH		VDDIO * 0.7			V
Input VIL				VDDIO * 0.3	V

[2] Values in this table do not include the effects of switching regulator ripple. The typical values represent default values that may be adjusted by software.

Parameter	Conditions	Min	Typ	Max	Unit
Drive Strength, push-pull high	VIO=VDDIO-0.3V				
	VDDIO = 3.3 V, PDSN=0		19		mA
	VDDIO = 3.3 V, PDSN=1		13		mA
	VDDIO = 3.3 V, PDSN=2		10		mA
	VDDIO = 3.3 V, PDSN=3		4		mA
	VDDIO = 1.8 V, PDSN=0		12		mA
	VDDIO = 1.8 V, PDSN=1		8		mA
	VDDIO = 1.8 V, PDSN=2		6		mA
	VDDIO = 1.8 V, PDSN=3		2		mA
Drive Strength, push-pull low	VIO is 0.3V				
	VDDIO = 3.3 V, PDSN=0		24		mA
	VDDIO = 3.3 V, PDSN=1		17		mA
	VDDIO = 3.3 V, PDSN=2		13		mA
	VDDIO = 3.3 V, PDSN=3		4		mA
	VDDIO = 1.8 V, PDSN=0		15		mA
	VDDIO = 1.8 V, PDSN=1		10		mA
	VDDIO = 1.8 V, PDSN=2		8		mA
	VDDIO = 1.8 V, PDSN=3		3		mA
Pull-up/down Resistance			145		kΩ

Table 2-6 Application ADC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
ADC Sample Resolution			16		bits
Input Voltage Range		0.05		0.55	V
Power Consumption (VBAT current at 3 V)	All other channels		400		µA
Measurement duration	2 MHz, 128-sample averaging		8		ms
	2 MHz, 32-sample averaging		2		

Parameter	Conditions	Min	Typ	Max	Unit
Effective Number of Bits[3]	Single-ended channel, 2 MHz, 32-sample averaging		11.4		bits
Signal to Noise and Distortion Ratio[3]	Single-ended channel, 2 MHz, 32-sample averaging		66.8		dB
Total Harmonic Distortion	Single-ended channel, 2 MHz, 32-sample averaging		-66.8		dB
Spurious Free Dynamic Range	Single-ended channel, 2 MHz, 32-sample averaging		68		dB
Integral Nonlinearity			+/- 1.2		LSB12
Differential Nonlinearity			+/- 1.5		LSB12
Gain Error			+/- 0.6		%
Offset Error			+/- 2		LSB12
Internal Temperature Sensor Accuracy	-40 to 85°C		+/- 2		°C

[3] The relationship between ENOB and SNDR is specified according to the standard ENOB calculator formula: ENOB = (SNDR - 1.76)/6.02

Table 2-7 SoC Power Consumption (3 V VBAT)

SoC Power Consumption **VBAT current at 3 V with internally generated I/O supply** (Active RX and Active Tx SoC Power Consumption includes Radio Power Consumption)					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Active RX	Sensitivity at: -95 dBm		 2.0		 mA
Active TX	Output power at: 0 dBm +4 dBm +8 dBm		 3.1 4.5 8.5		 mA mA mA
MCU Active (32 MHz)	Executing CoreMark from RAM at 32 MHz		1.8		mA
MCU Active (64 MHz)	Executing CoreMark from RAM at 64 MHz		3.5		mA
MCU Idle + Radio Deep Sleep			0.4		mA
Retention	0 KB SRAM 32 KB SRAM 128 KB SRAM 256 KB SRAM		1.5 1.6 2.0 2.4		µA µA µA µA
Hibernation			1.1		µA
SoC Off with Analog Comparator			450		nA
SoC Off			300		nA
Powerdown	PWD pin asserted		100		nA

Table 2-8 Flash Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VDDIO		1.62	1.8	3.6	V
Endurance		100000			Cycles
Data Retention		20			Years
Read Cycle	VDDIO Current @ 1.8 V Duration (4 bytes at 32 MHz)		2.0 1.0		mA µs
Write Cycle Pattern: 0x55 -> 0xaa	VDDIO Current @ 1.8 V Duration (4 bytes at 32 MHz)		2.7 1.7		mA µs

3 Pinout Description

3.1 ATM5305 and ATM5205 4x4 mm, 93-ball BGA Pinout

The ATM5305 4x4 mm and ATM5205 5x5 versions are packaged in a No Lead, 93-ball Ball Grid Array Flat Package (BGA). The pin assignment is shown in Table 3.1-1. All pins are on the bottom side of the package.

Figure 3.1-1 ATM5305 and ATM5205 4x4 mm, 93-ball BGA Pinout (Top View)

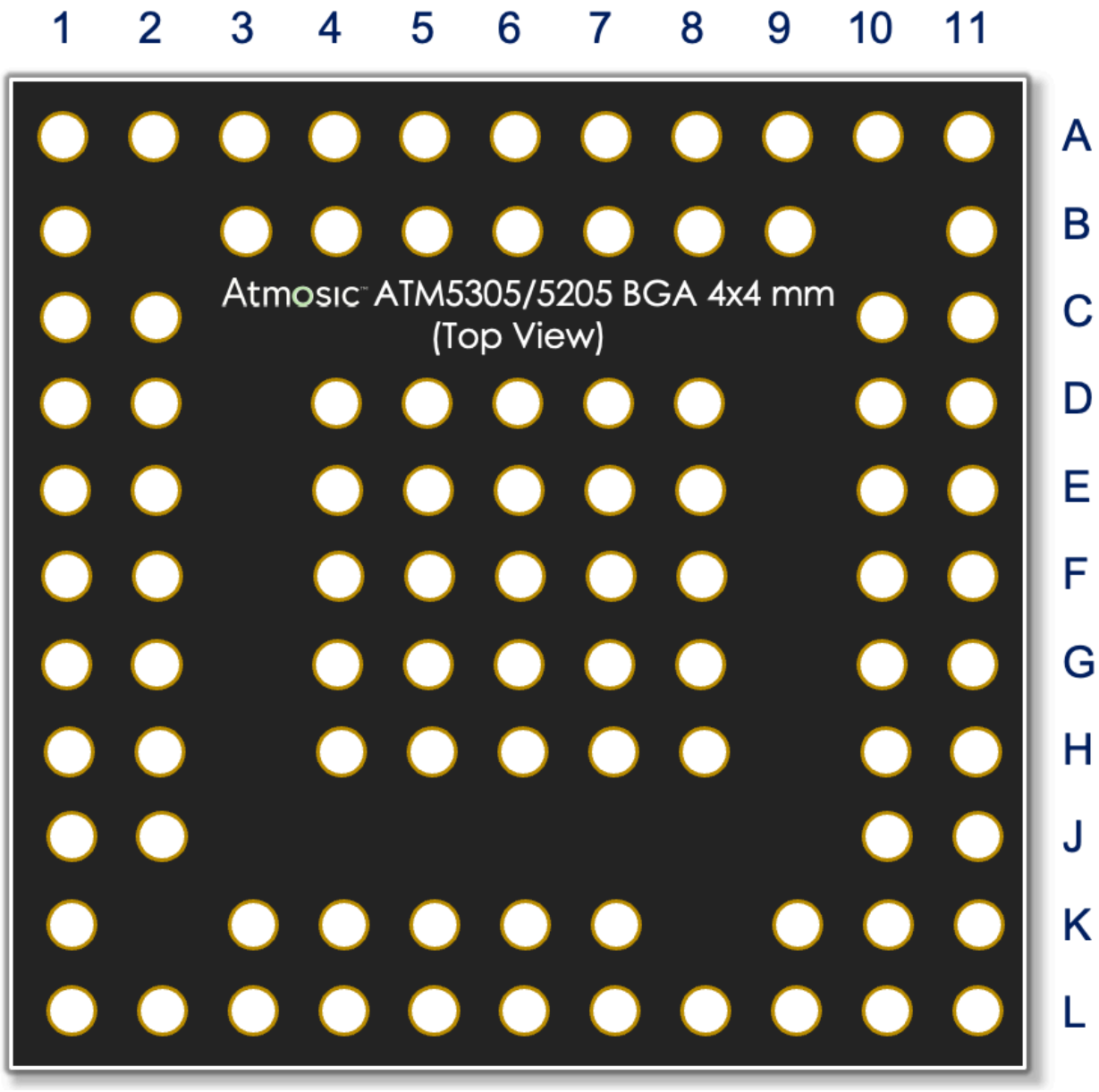
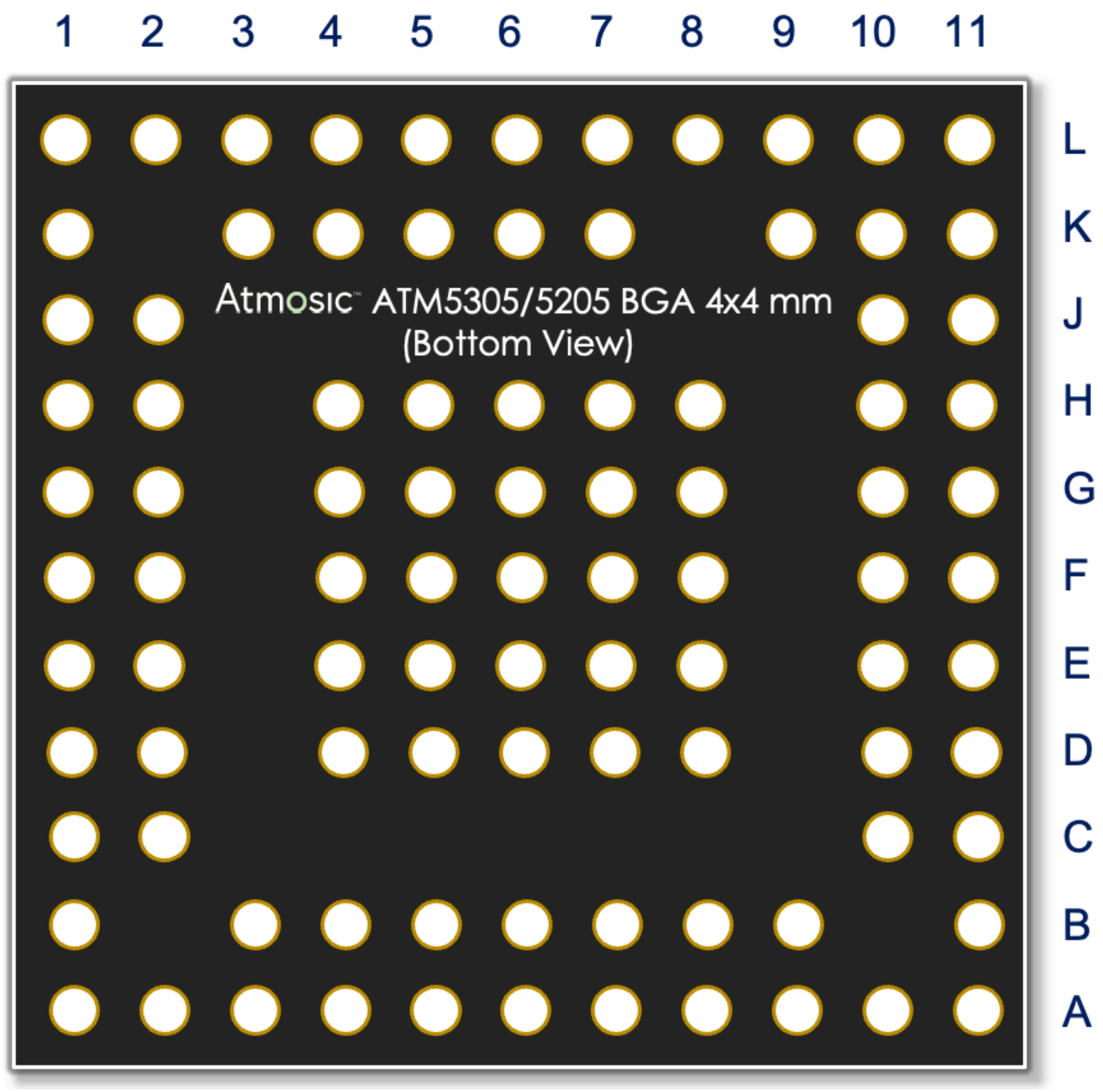


Figure 3.1-2 **ATM5305 and ATM5205 4x4 mm, 93-ball BGA Pinout (Bottom View)**



Pin Type Definitions	
Pin Type	**Definition**
I/O	Signal Input Output
RF	Radio Frequency
PWR	Power supply
A	Analog
R	Reserved
NC	No connection, must be open
GND	Ground

Table 3.1-1 ATM5305 and ATM5205 4x4 mm, 93-ball BGA Pin Description

ATM5305 4x4 mm, 93-ball BGA Description			
Ball Number	**Name**	**Type**	**Description**
A1	RFIO	RF	2.4 GHz Single-ended RF I/O for Bluetooth radio
A2	VBAT1V_RF	PWR	Radio power supply
A3	P47	I/O	Programmable Digital I/O
A4	P45	I/O	Programmable Digital I/O
A5	XTALO_32M	A	32 MHz crystal oscillator output
A6	XTALI_32M	A	32 MHz crystal oscillator input
A7	VDDIO	PWR	Digital and Analog I/O Power Supply
A8	P38	I/O	Programmable Digital I/O or Analog Input
A9	P37	I/O	Programmable Digital I/O or Analog Input
A10	RES	R	Reserved, must tie to ground
A11	VBAT1V	PWR	1.5V power supply (VBAT_MODE = 0) or switching regulator output (VBAT_MODE = 1)
B1	VDDPA	PWR	PA power supply
B3	P46	I/O	Programmable Digital I/O
B4	P44	I/O	Programmable Digital I/O
B5	P43	I/O	Programmable Digital I/O or Analog Input
B6	P42	I/O	Programmable Digital I/O or Analog Input
B7	P41	I/O	Programmable Digital I/O or Analog Input
B8	P40	I/O	Programmable Digital I/O or Analog Input
B9	P39	I/O	Programmable Digital I/O or Analog Input and SOCOFF_WAKE
B11	VSS	GND	Ground supply for all circuits
C1	P0	I/O	Programmable Digital I/O and SWDCLK

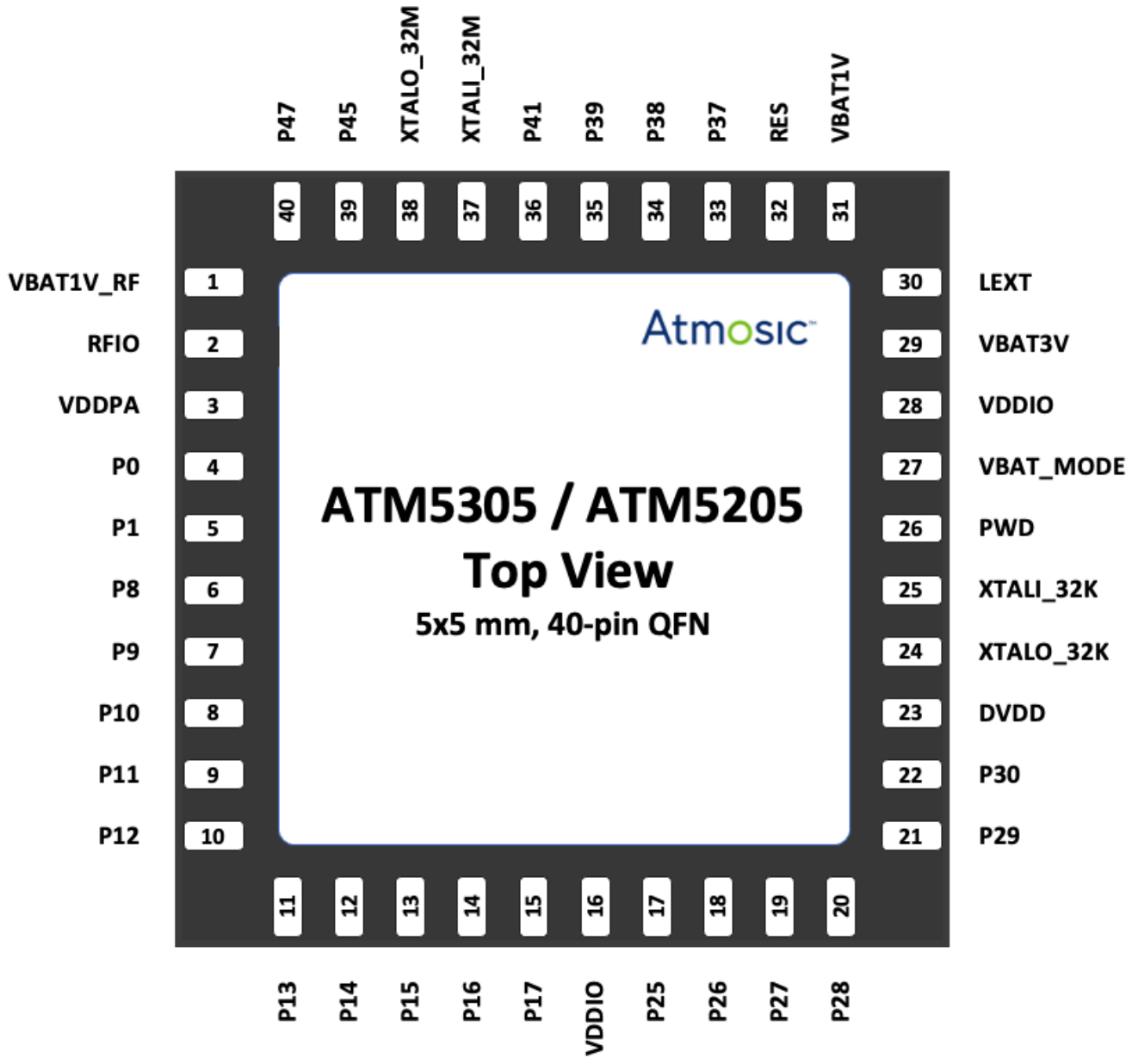
C2	P1	I/O	Programmable Digital I/O and SWDIO
C10	VSS	GND	Ground supply for all circuits
C11	LEXT	A	Switcher Inductor
D1	P2	I/O	Programmable Digital I/O
D2	P3	I/O	Programmable Digital I/O
D4	VSS	GND	Ground supply for all circuits
D5	VSS	GND	Ground supply for all circuits
D6	VSS	GND	Ground supply for all circuits
D7	VSS	GND	Ground supply for all circuits
D8	VSS	GND	Ground supply for all circuits
D10	VSS	GND	Ground supply for all circuits
D11	VBAT3V	PWR	3V power supply (VBAT_MODE = 1) or switching regulator output (VBAT_MODE = 0)
E1	P4	I/O	Programmable Digital I/O
E2	P5	I/O	Programmable Digital I/O
E4	VSS	GND	Ground supply for all circuits
E5	VSS	GND	Ground supply for all circuits
E6	VSS	GND	Ground supply for all circuits
E7	VSS	GND	Ground supply for all circuits
E8	VSS	GND	Ground supply for all circuits
E10	VBAT_MODE	I/O	VBAT power mode selection (0: VBAT = VBAT1V; 1: VBAT = VBAT3V)
E11	VDDIO	PWR	Digital and Analog I/O Power Supply
F1	P6	I/O	Programmable Digital I/O
F2	P7	I/O	Programmable Digital I/O
F4	VSS	GND	Ground supply for all circuits
F5	VSS	GND	Ground supply for all circuits
F6	VSS	GND	Ground supply for all circuits
F7	VSS	GND	Ground supply for all circuits
F8	VSS	GND	Ground supply for all circuits
F10	PWD	I/O	Power Down Input (Active High)
F11	XTALI_32K	A	32.768 kHz crystal oscillator input
G1	P8	I/O	Programmable Digital I/O
G2	P9	I/O	Programmable Digital I/O
G4	VSS	GND	Ground supply for all circuits
G5	VSS	GND	Ground supply for all circuits
G6	VSS	GND	Ground supply for all circuits
G7	VSS	GND	Ground supply for all circuits
G8	VSS	GND	Ground supply for all circuits
G10	P36	I/O	Programmable Digital I/O
G11	XTALO_32K	A	32.768 kHz crystal oscillator output
H1	P10	I/O	Programmable Digital I/O
H2	P11	I/O	Programmable Digital I/O
H4	VSS	GND	Ground supply for all circuits

H5	VSS	GND	Ground supply for all circuits
H6	VSS	GND	Ground supply for all circuits
H7	VSS	GND	Ground supply for all circuits
H8	VSS	GND	Ground supply for all circuits
H10	P35	I/O	Programmable Digital I/O
H11	DVDD	PWR	Digital core power supply
J1	P12	I/O	Programmable Digital I/O
J2	P13	I/O	Programmable Digital I/O
J10	P33	I/O	Programmable Digital I/O
J11	P34	!/O	Programmable Digital I/O
K1	P14	I/O	Programmable Digital I/O
K3	P17	I/O	Programmable Digital I/O
K4	P19	I/O	Programmable Digital I/O
K5	P21	I/O	Programmable Digital I/O
K6	P22	I/O	Programmable Digital I/O
K7	P24	I/O	Programmable Digital I/O
K9	P27	I/O	Programmable Digital I/O
K10	P31	I/O	Programmable Digital I/O
K11	P32	I/O	Programmable Digital I/O
L1	P15	I/O	Programmable Digital I/O
L2	P16	I/O	Programmable Digital I/O
L3	P18	I/O	Programmable Digital I/O
L4	P20	I/O	Programmable Digital I/O
L5	VDDIO	PWR	Digital and Analog I/O Power Supply
L6	P23	I/O	Programmable Digital I/O
L7	P25	I/O	Programmable Digital I/O
L8	P26	I/O	Programmable Digital I/O
L9	P28	I/O	Programmable Digital I/O
L10	P29	I/O	Programmable Digital I/O
L11	P30	I/O	Programmable Digital I/O

3.2 ATM5305 and ATM5205 5x5 mm, 40-pin QFN Pinout

The ATM5305 and ATM5205 5x5 mm versions are packaged in a No Lead, 40-pin Quad Flat Package (QFN). The pin assignment is shown in Table 3.2-1. All pins are on the bottom side of the package.

Figure 3.2-1 ATM5305 and ATM5205 5x5 mm, 40-pin QFN Pinout (Top View)



Pin Type Definitions	
Pin Type	**Definition**
I/O	Signal Input Output
RF	Radio Frequency
PWR	Power supply
A	Analog
R	Reserved
NC	No connection, must be open
GND	Ground

Table 3.2-1 ATM5305 and ATM5205 5x5 mm, 40-pin QFN Pin Description

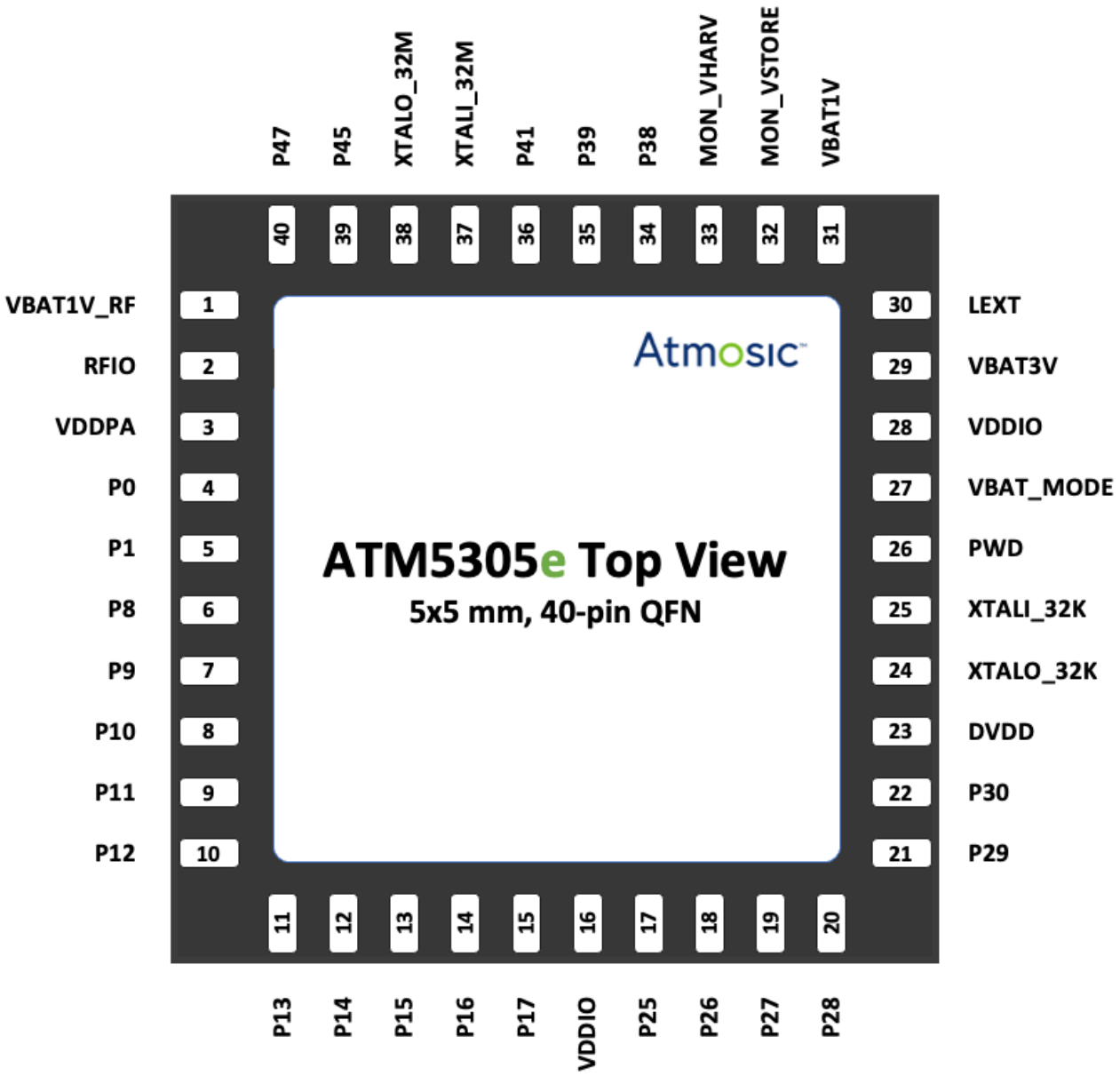
ATM5305 and ATM5205 5x5 mm, 40-pin QFN Pin Description			
Pin Number	**Name**	**Type**	**Description**
1	VBAT1V_RF	PWR	Radio power supply
2	RFIO	RF	2.4 GHz Single-ended RF I/O for Bluetooth radio
3	VDDPA	PWR	PA power supply
4	P0	I/O	Programmable Digital I/O and SWDCLK
5	P1	I/O	Programmable Digital I/O and SWDIO
6	P8	I/O	Digital and Analog I/O Power Supply
7	P9	I/O	Programmable Digital I/O
8	P10	I/O	Programmable Digital I/O
9	P11	I/O	Programmable Digital I/O
10	P12	I/O	Programmable Digital I/O
11	P13	I/O	Programmable Digital I/O
12	P14	I/O	Programmable Digital I/O
13	P15	I/O	Programmable Digital I/O
14	P16	I/O	Programmable Digital I/O
15	P17	I/O	Programmable Digital I/O
16	VDDIO	PWR	Digital and Analog I/O Power Supply
17	P25	I/O	Programmable Digital I/O
18	P26	I/O	Programmable Digital I/O
19	P27	I/O	Programmable Digital I/O
20	P28	I/O	Programmable Digital I/O
21	P29	I/O	Programmable Digital I/O

22	P30	I/O	Programmable Digital I/O
23	DVDD	PWR	Digital core power supply
24	XTALO_32K	A	32.768 kHz crystal oscillator output
25	XTALI_32K	A	32.768 kHz crystal oscillator input
26	PWD	I/O	Power Down Input (Active High)
27	VBAT_MODE	I/O	VBAT power mode selection (0: VBAT = VBAT1V; 1: VBAT = VBAT3V)
28	VDDIO	PWR	Digital and Analog I/O Power Supply
29	VBAT3V	PWR	3V power supply (VBAT_MODE = 1) or switching regulator output (VBAT_MODE = 0)
30	LEXT	A	Switcher Inductor
31	VBAT1V	PWR	1.5V power supply (VBAT_MODE = 0) or switching regulator output (VBAT_MODE =1)
32	RES	R	Reserved, must tie to ground
33	P37	I/O	Programmable Digital I/O or Analog Input
34	P38	I/O	Programmable Digital I/O or Analog Input
35	P39	I/O	Programmable Digital I/O or Analog Input and SOCOFF_WAKE
36	P41	I/O	Programmable Digital I/O or Analog Input
37	XTALI_32M	A	32 MHz crystal oscillator input
38	XTALO_32M	I/O	32 MHz crystal oscillator output
39	P45	I/O	Programmable Digital I/O
40	P47	I/O	Programmable Digital I/O
EPAD	VSS	GND	Ground supply for all circuits. The 40-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS.

3.3 ATM5305e 5x5 mm, 40-pin QFN Pinout

The ATM5305e 5x5 mm version is packaged in a No Lead, 40-pin Quad Flat Package (QFN). The pin assignment is shown in Table 3.3-1. All pins are on the bottom side of the package.

Figure 3.3-1 ATM5305e 5x5 mm, 40-pin QFN Pinout (Top View)



Pin Type Definitions	
Pin Type	**Definition**
I/O	Signal Input Output
RF	Radio Frequency
PWR	Power supply
A	Analog
R	Reserved
NC	No connection, must be open
GND	Ground

Table 3.3-1 ATM5305e 5x5 mm, 40-pin QFN Pin Description

ATM5305e 40-pin QFN Pin Description			
Pin Number	**Name**	**Type**	**Description**
1	VBAT1V_RF	PWR	Radio power supply
2	RFIO	RF	2.4 GHz Single-ended RF I/O for Bluetooth radio
3	VDDPA	PWR	PA power supply
4	P0	I/O	Programmable Digital I/O and SWDCLK
5	P1	I/O	Programmable Digital I/O and SWDIO
6	P8	I/O	Digital and Analog I/O Power Supply
7	P9	I/O	Programmable Digital I/O
8	P10	I/O	Programmable Digital I/O
9	P11	I/O	Programmable Digital I/O
10	P12	I/O	Programmable Digital I/O
11	P13	I/O	Programmable Digital I/O
12	P14	I/O	Programmable Digital I/O
13	P15	I/O	Programmable Digital I/O
14	P16	I/O	Programmable Digital I/O
15	P17	I/O	Programmable Digital I/O
16	VDDIO	PWR	Digital and Analog I/O Power Supply
17	P25	I/O	Programmable Digital I/O
18	P26	I/O	Programmable Digital I/O
19	P27	I/O	Programmable Digital I/O
20	P28	I/O	Programmable Digital I/O
21	P29	I/O	Programmable Digital I/O

22	P30	I/O	Programmable Digital I/O
23	DVDD	PWR	Digital core power supply
24	XTALO_32K	A	32.768 kHz crystal oscillator output
25	XTALI_32K	A	32.768 kHz crystal oscillator input
26	PWD	I/O	Power Down Input (Active High)
27	VBAT_MODE	I/O	VBAT power mode selection (0: VBAT = VBAT1V; 1: VBAT = VBAT3V)
28	VDDIO	PWR	Digital and Analog I/O Power Supply
29	VBAT3V	PWR	3V power supply (VBAT_MODE = 1) or switching regulator output (VBAT_MODE = 0)
30	LEXT	A	Switcher Inductor
31	VBAT1V	PWR	1.5V power supply (VBAT_MODE = 0) or switching regulator output (VBAT_MODE = 1)
32	MON_VSTORE	A	External energy storage monitoring for energy harvesting. Should be be grounded if energy harvesting is not used
33	MON_VHARV	A or I/O	External energy source monitoring for energy harvesting. Can also be configured as Programmable Digital I/O or Analog Input when Energy Harvesting is disabled.
34	P38	I/O	Programmable Digital I/O or Analog Input
35	P39	I/O	Programmable Digital I/O or Analog Input and SOCOFF_WAKE
36	P41	I/O	Programmable Digital I/O or Analog Input
37	XTALI_32M	A	32 MHz crystal oscillator input
38	XTALO_32M	I/O	32 MHz crystal oscillator output
39	P45	I/O	Programmable Digital I/O
40	P47	I/O	Programmable Digital I/O
EPAD	VSS	GND	Ground supply for all circuits. The 40-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS.

4 Mechanical Drawing

4.1 ATM5305 and ATM5205 4x4 mm, 93-ball BGA Package

Figure 4.1-1 ATM5305 and ATM5205 4x4 mm, 93-ball BGA Mechanical Drawing

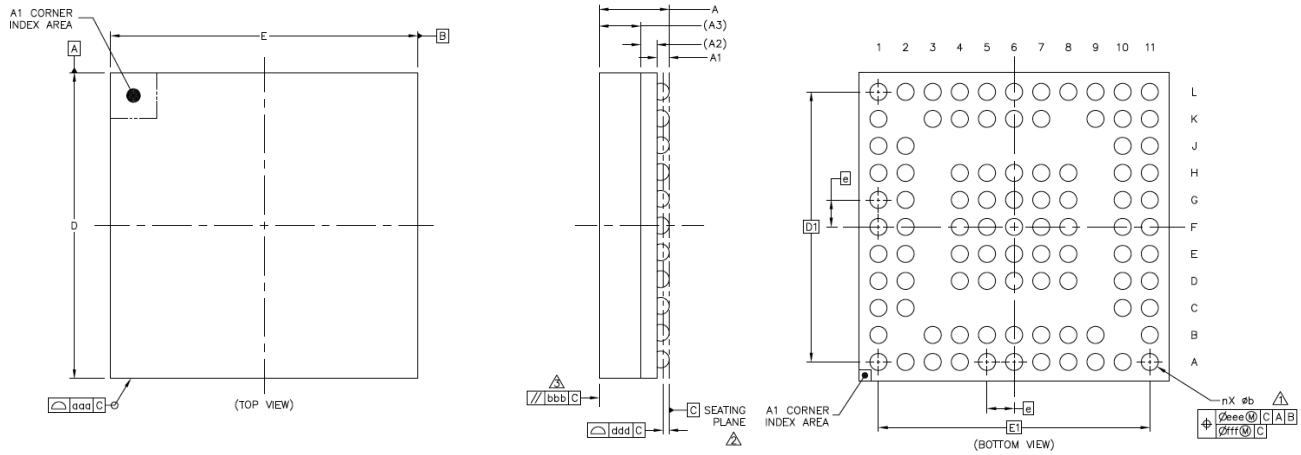


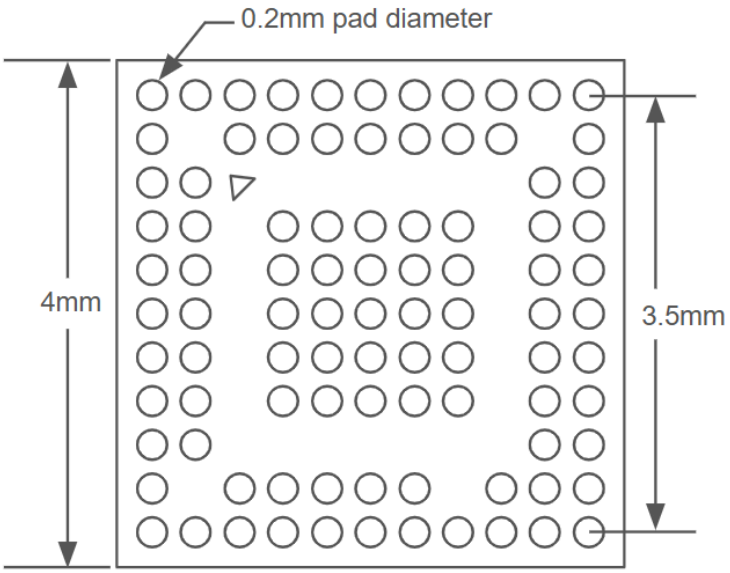
Table 4.1-1 ATM5305 and ATM5205 4x4 mm, 93-ball BGA Dimensions

		Symbol	Min	Nom	Max
Total Thickness		A	0.835	0.91	1
Stand Off		A1	0.12	-	0.2
Substrate Thickness		A2	0.21 REF		
Mold Thickness		A3	0.54 REF		
Body Size	X	D	3.9	4	4.1
	Y	E	3.9	4	4.1
Ball Diameter		b	0.17	0.22	0.27
Ball Pitch		e	0.35 BSC		
Edge Ball Center to Center	X	D1	3.5 BSC		
	Y	E1	3.5 BSC		
Package Edge Tolerance		aaa	0.1		
Mold Flatness		bbb	0.1		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.08		

Notes:

1. All dimensions are in millimeters.
2. Coplanarity applies to leads, corner leads, and die-attached pads.
3. Soldering of 0.35mm ball pitch for the BGA package requires controlled reflow soldering processes. Utilization of the hand soldering process is not recommended. For optimal results, customers should consult their assembly partners.

Figure 4.1-2 ATM5305 and ATM5205 4x4 mm, 93-ball BGA Landing Pattern (Top View)



Notes:

1. All dimensions are in millimeters (mm) unless otherwise noted.
2. The land pattern is based on the IPC-7351 guidelines. There may be other options specified in that publication.
3. The notes above and the land pattern are recommendations only. Customers may need to use different parameters as required for their application, materials, SMT process, and tooling requirements.

4.2 ATM5305 / ATM5305e / ATM5205, 5x5 mm, 40-pin QFN Package

Figure 4.2-1 ATM5305 / ATM5305e / ATM5205 5x5 mm, 40-pin QFN Mechanical Drawing

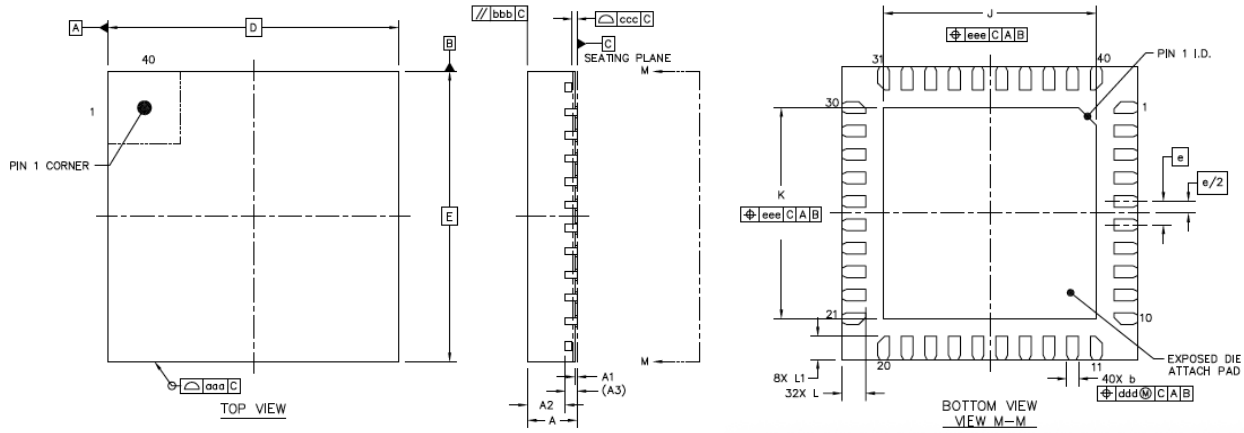


Table 4.2-1 ATM5305 / ATM5305e / ATM5205 5x5 mm, 40-pin QFN Dimensions

		Symbol	Min	Nom	Max
Total Thickness		A	0.8	0.85	0.9
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	---	0.65	---
L/F Thickness		A3	0.203 REF		
Lead Width		b	0.15	0.2	0.25
Body Size	X	D	5 BSC		
	Y	E	5 BSC		
Lead Pitch		e	0.4 BSC		
EP Size	X	J	3.5	3.6	3.7
	Y	K	3.5	3.6	3.7
Lead Length		L	0.35	0.4	0.45
		L1	0.3	0.4	0.45
Package Edge Tolerance		aaa	0.1		
Mold Flatness		bbb	0.1		
Coplanarity		ccc	0.08		
Lead Offset		ddd	0.1		
Exposed Pad Offset		eee	0.1		

Notes:

1. All dimensions are in millimeters.
2. Coplanarity applies to leads, corner leads, and die-attached pads.

Figure 4.2-2 ATM5305 / ATM5305e / ATM5205 5x5 mm, 40-pin QFN Landing Pattern

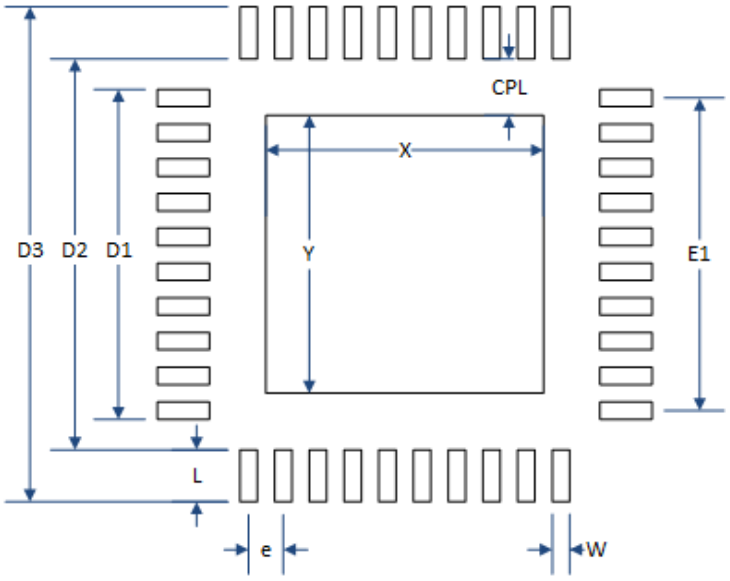


Table 4.2-2 ATM5305 / ATM5305e / ATM5205 5x5 mm, 40-pin QFN Land Pattern Dimensions

Symbol	Typ
CPL	0.65
D1	3.8
D2	4.5
D3	5.7
e	0.4
E1	3.6
L	0.6
W	0.2
X	3.2
Y	3.2

Notes:

1. All dimensions are in millimeters (mm) unless otherwise noted.
2. The land pattern is based on the IPC-7351 guidelines. There may be other options specified in that publication.
3. The notes above and the land pattern are recommendations only. Customers may need to use different parameters as required for their application, materials, SMT process, and tooling requirements.

4.3 Solder Reflow Profile

The recommended reflow profile is per the IPC/JEDEC J-STD-020 specification for all the packages listed in Mechanical Drawing. Please obtain the official specifications from JEDEC (https://www.jedec.org/).

4.4 Manual Soldering / Hot Soldering

Utilization of the manual soldering process is not recommended. For optimal results, customers should consult their assembly partners.

5 Part Ordering

Table 5-1 Part Ordering Numbers

Part Ordering Number	Product Line	Description	Channel Sounding	Energy Harvesting	GPIO	Maximum Number of General-Purpose Peripherals[4]					
						GADC (general single-ended channels listed)	UART	SPI	I^2S	I^2C	PWM
ATM5305-3NC8BV-SR	ATM53 Bluetooth 6.3 Wireless MCU	ATM53 Series Bluetooth 6.3 Wireless MCU, **4x4 mm BGA 93 ball**, without energy-harvesting or wake-up receiver (WuRX), **2048KB NVM**, 256KB SRAM, Operating Temperature -40 °C to 85 °C, Small Reel, 7" 1K devices/reel	Y	N	48	7	3	2	1	2	8
ATM5305-3NC8BV	ATM53 Bluetooth 6.3 Wireless MCU	ATM53 Series Bluetooth 6.3 Wireless MCU, **4x4 mm BGA 93 ball**, without energy-harvesting or wake-up receiver (WuRX), **2048KB NVM**, 256KB SRAM), Operating Temperature -40 °C to 85 °C, sampling quantity in a tray, not for production volume	Y	N	48	7	3	2	1	2	8

[4] Actual peripherals available depending on Pin Multiplexing configuration. Please refer to Pin Multiplexing for details.

Part Ordering Number	Product Line	Description			GPIO	Maximum Number of General-Purpose Peripherals[4]					
						GADC (general single-ended channels listed)	UART	SPI	I^2S	I^2C	PWM
ATM5305-3NC8QK-SR	ATM53 Bluetooth 6.3 Wireless MCU	ATM53 Series Bluetooth 6.3 Wireless MCU, **5x5 mm QFN 40 pin**, without energy-harvesting, **2048KB NVM**, 256KB SRAM, Operating Temperature -40 °C to 85 °C, Small Reel, 7” 1K devices/reel	Y	N	24	4	3	2	1	2	8
ATM5305-3NC8QK	ATM53 Bluetooth 6.3 Wireless MCU	ATM53 Series Bluetooth 6.3 Wireless MCU, **5x5 mm QFN 40 pin**, without energy-harvesting, **2048KB NVM**, 256KB SRAM, Operating Temperature -40 °C to 85 °C, sampling quantity in a tray, not for production volume	Y	N	24	4	3	2	1	2	8
ATM5205-3NC8BV-SR	ATM52 Bluetooth 5.4 Wireless MCU	ATM52 Series Bluetooth 5.4 Wireless MCU, **4x4 mm BGA 93 ball**, without energy-harvesting or wake-up receiver (WuRX), **2048KB NVM**, 256KB SRAM, Operating Temperature -40 °C to 85 °C, Small Reel, 7” 1K devices/reel	N	N	48	7	3	2	1	2	8
ATM5205-3NC8BV	ATM52 Bluetooth 5.4 Wireless MCU	ATM52 Series Bluetooth 5.4 Wireless MCU, **4x4 mm BGA 93 ball**, without energy-harvesting or wake-up receiver (WuRX), **2048KB NVM**,	N	N	48	7	3	2	1	2	8

Part Ordering Number	Product Line	Description			GPIO	Maximum Number of General-Purpose Peripherals[4]					
						GADC (general single-ended channels listed)	UART	SPI	I^2S	I^2C	PWM
		256KB SRAM), Operating Temperature -40 °C to 85 °C, sampling quantity in a tray, not for production volume									
ATM5205-3NC8QK-SR	ATM52 Bluetooth 5.4 Wireless MCU	ATM5 Series Bluetooth 5.4 Wireless MCU, **5x5 mm QFN 40 pin**, without Bluetooth Channel Sounding, without energy-harvesting, **2048KB NVM**, 256KB SRAM, Operating Temperature -40 °C to 85 °C, Small Reel, 7” 1K devices/reel	N	N	24	4	3	2	1	2	8
ATM5205-3NC8QK	ATM52 Bluetooth 5.4 Wireless MCU	ATM5 Series Bluetooth 5.4 Wireless MCU, **5x5 mm QFN 40 pin**, without Bluetooth Channel Sounding, without energy-harvesting, **2048KB NVM**, 256KB SRAM, Operating Temperature -40 °C to 85 °C, sampling quantity in a tray, not for production volume	N	N	24	4	3	2	1	2	8

Part Ordering Number	Product Line	Description			GPIO	Maximum Number of General-Purpose Peripherals[4]					
						GADC (general single-ended channels listed)	UART	SPI	I^2S	I^2C	PWM
ATM5305E-2NC8QK-SR	ATM53 Bluetooth 6.3 Wireless MCU	ATM5 Series Bluetooth 6.3 Wireless MCU, **5x5 mm QFN 40 pin, with energy-harvesting, 2048KB NVM**, 256KB SRAM, Operating Temperature -40 °C to 85 °C, Small Reel, 7" 1K devices/reel	Y	Y	24[5]	4[6]	3	2	1	2	8
ATM5305E-2NC8QK	ATM53 Bluetooth 6.3 Wireless MCU	ATM5 Series Bluetooth 6.3 Wireless MCU, **5x5 mm QFN 40 pin, with energy-harvesting, 2048KB NVM**, 256KB SRAM, Operating Temperature -40 °C to 85 °C, sampling quantity in a tray, not for production volume	Y	Y	24[6]	4[7]	3	2	1	2	8

[5] When Energy Harvesting is enabled, this package has 23 GPIOs; when Energy Harvesting is disabled, this package has 24 GPIOs
[6] When Energy Harvesting is enabled, this package has 3 GADC single-ended channels; when Energy Harvesting is disabled, this package has 4 GADC single-ended channels

Reference Documents

Document Title	Description	Link
Arm® TrustZone Technology for the Armv8-M Architecture v2.1	TrustZone Architecture Manual	https://developer.arm.com/documentation
Arm® Cortex®-M33 Devices Generic User Guide Revision r1p0	Cortex M33 Users Guide	https://developer.arm.com/documentation
ARM®v8-M Architecture Reference Manual ARM DDI 0553A.e	ARMv8-M Core architecture reference	https://developer.arm.com/documentation

Revision History

Date	Version	Description
September 18, 2026	0.18	Updated Part Ordering Numbers
September 10, 2026	0.11	Updated PMU External Pins, Peripherals and I/O, Recommended Operating Conditions, Radio Transceiver Characteristics, Application ADC Characteristics, SoC Power Consumption (3 V VBAT), Flash Characteristics, Part Ordering Numbers
June 17, 2026	0.10	Initial release.

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